1. Mark the **true** statements **with** an **X** and the **false** statements **with a –** in the last column. Each good answer is 0.5 points, each wrong answer -0.5 points, and an empty answer 0 point. Total of 0 to 3 points.		
The Neumann architecture computer stores the instructions and data in the same memory, and in the same format.		**(3*p*)**
The CPU can use a microprogrammed control unit for faster instruction execution.		
In a multitasking system, each task is assigned to an individual physical processor.		
The Cache is used to make the memory apparently faster to the user.		
The Cache makes data transfer between the virtual and physical memory faster.		
A Harward architecture computer can be faster because it can read from two memories at the same time.		

2. Mark the **true** statements **with** an **X** and the **false** statements **with a –** in the last column. Each good answer is 0.5 points, each wrong answer -0.5 points, and an empty answer 0 point. Total of 0 to 3 points.		
A zero address machine always needs to have a stack.		**(3*p*)**
A four address machine has to have a program counter.		
Tasks on an x86 based system can call themselves (can be recursive).		
During a task switch, the internal state of the processor is saved entirely by sofware.		
The Task State Segment (TSS) is a descriptor data structure that stores the actual state of a task's execution.		
In case of the x86, the number of bits used to indicate the starting address of a page does not depend on the actually implemented size of the physical memory.		

3. What is the purpose of a TASK GATE in the x86 architecture?

(2*p*)

4. Which descriptor tables can contain CALL GATEs in the x86 architecture?

(1*p*)

5. A cache uses a **4 way set associative mapping** scheme. The block size is 256 bytes, the whole cache stores 1024 blocks. There **is one extra bit** in the control stores to indicate validity of each block. The physical address is 32 bits long.

(5*p*)

a) **How long is the offset** part of the address?

b) **What is the organization of a Control Store** (words x bits)? (2 points)

c) **How many TAG comparators** are there in the cache?

6. Draw the signal pattern of the writing current in case of PE, FM and MFM modulation

(3*p*)

0…0	1	1	0	0	1
PE					
FM					
MFM					

7. A system has an operative memory with $\mathbf{T_L}$**=70ns** access time. A 128KB **set associative cache** memory is used in this system **with an access time of 10ns**. The **hit rate** is **90%**.

(*2p*)

a) **Give the average effective access time as visible to the user** if the block load time would be **200ns.**

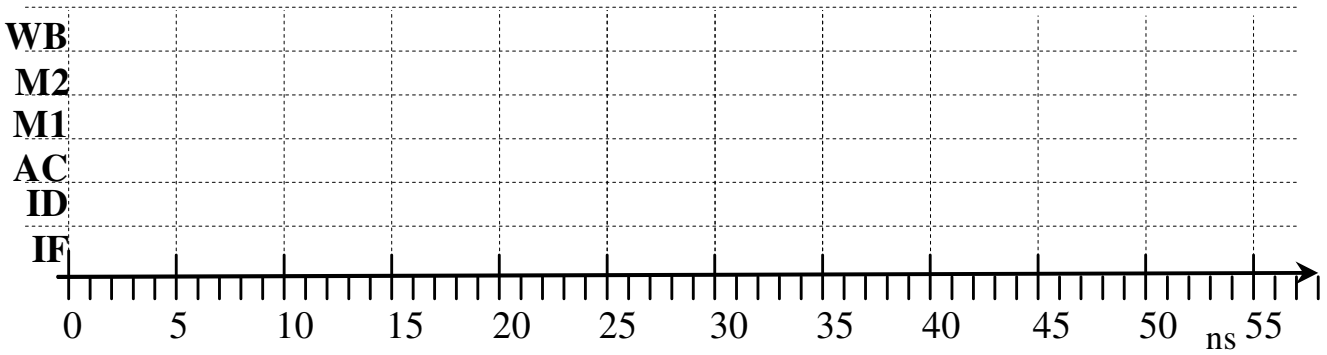
b) How fast cache memory is needed in order to **lower the effective access time to 14ns**?

8. Given is a pipeline system with synchronous scheduling and 6 elementary operations. The elementary operations have the following execution times: **IF: 6.5ns, ID: 4.5ns, AC=4.5ns, M1=8.5ns, M2=5.5ns, and WB=6.5ns**

(*6p*)

Because of the synchronous operation, **each** elementary execution **unit** needs an **additional 0.5ns to transfer its result** to the next unit, **even the last one** needs this time to output the result.

Draw the execution timing diagram in the following figure. (2 points)
Mark the waiting times (e.g. like this: ▨**).**



How long is the latency? (1 point)

Give the value of the restart time. (1 point)

Give the efficiency of the pipeline. (2 point)

9. A computer system uses an **index register** memory extension system. **The logical address space is 64KBytes, the physical address space** (memory size) **is 256KBytes**. The first 4 bits of the logical address are used as index. Additional 2 bits are used for control (they are before the address extension bits). **(5*p*)**

Draw the layout of the index register array (1 point).

Give the **size (number of registers, number of bits) of the index register array.** (2 points)

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In this system, we want to run **a program** that is compiled **to start at address (63FFh)** and has **a size** of **8KBytes**. **Which register(s)** do we need **to set** in the index register array? (1 point)

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In the physical memory, there **is free** space **between 17000h and 17FFFh** (4KB space) and **after 30000h** up to the end of physical memory (3FFFFh).
What value(s) should we set to the given index registers? (there are many possible good answers) (1 point)

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