Budapest University of Technology and Economics
Department of Electron Devices

Technology of IT Devices

Lecture 1

- Lecturers and Administration
- Course Requirements
- Lab Timing and Softwares
- Course Topics/Syllabus
- Basic Concepts of Semiconductors
- Microelectronics & Integrated Circuits IC's
- Trends in Integrated Circuit Technology

Lecturers and Administration

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- The course can be found on EDU: Edu.vik.bme.hu

PLEASE DO NOT RECORD THE LECTURES!

Course Requirements

- Five computer laboratories
  - They will be marked as pass or fail.
  - One lab can be retaken.
- One midterm test at the end of this semester (in-person)
  - It also can be retaken.
- You must pass both the labs and the midterm test to pass this course.
- Final grade will be calculated, based on the result of the midterm test:
  - 0-40% : fail (1)
  - 41-55%: satisfactory (2)
  - 56-70%: average (3)
  - 71-85%: good (4)
  - 86-100%: excellent (5)

Lab Timing and Softwares

- There will be Five labs on odd weeks (please check the time table).
- The first lab will be on September 24th (Friday).
- The lab materials will be uploaded to EDU too.

- LTspice
  - For basic analog and digital circuits

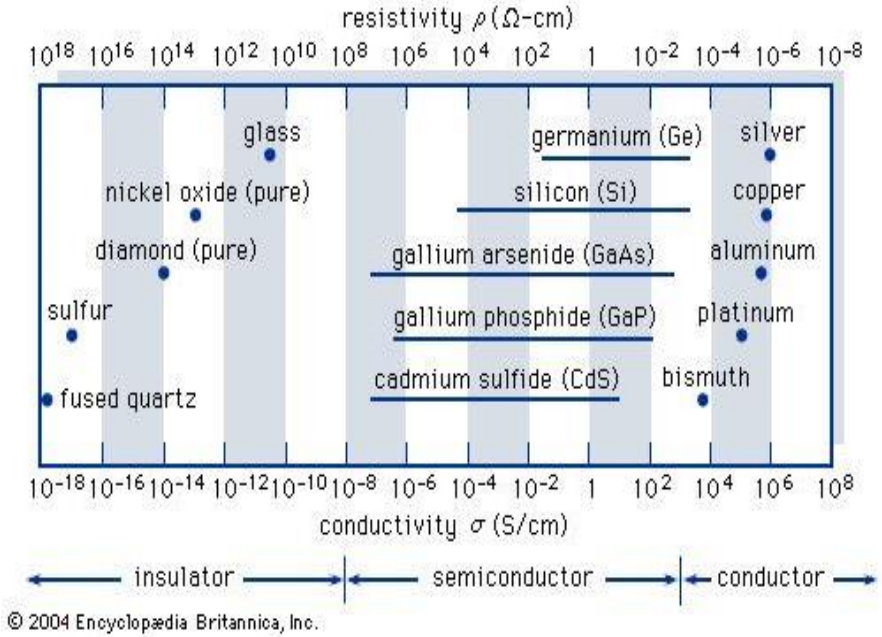
- FloTerm
  - For basic analog and digital circuits

Course Topics/Syllabus

1. Microelectronics and IC Introduction
2. Microelectronics (CMOS)
3. IC Manufacturing Technology
4. IC Packaging_1
5. IC Packaging _2
6. Parasitic effects of packaging
7. Thermal effects on IC packaging_1
8. Thermal effects on IC packaging_2
9. Design flow of electrical equipment
10. Introduction to signal integrity_1
11. Introduction to signal integrity_2

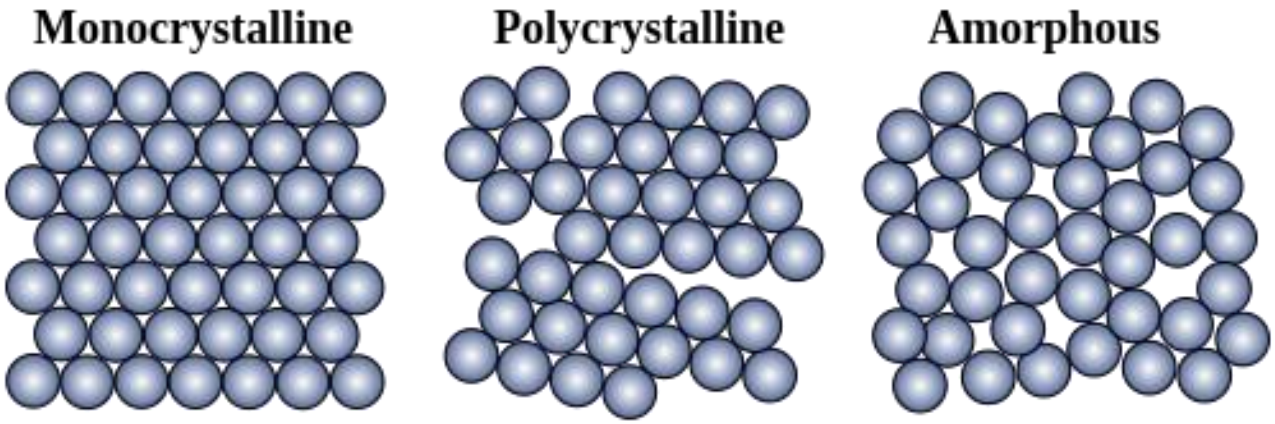
Basic Concepts of Semiconductors

- What does semiconductor mean?
- What material are transistors made of?
- How does it work?
- Why is it suitable to create a logic gate?
- Semiconductors' conductance is between that of conductors and insulators



- They conduct current
  - Semiconductors have a negative thermal coefficient (NTC)
    - It means their conductivity increases when temperature rises.
    - This is exactly the opposite behaviour of metals.
- The most important semiconductors:
  - Monocrystalline or single-crystal materials:
    - Semiconductor elements: Si (silicon), Ge (germanium)
    - Compound semiconductors: GaAs (gallium arsenide), GaAsP (gallium arsenide phosphide). They are used to create LEDs.
  - Amorphous semiconductors: amorphous Si mainly
- Organic semiconductors: OLEDs (Organic LEDs)

Types of Crystal

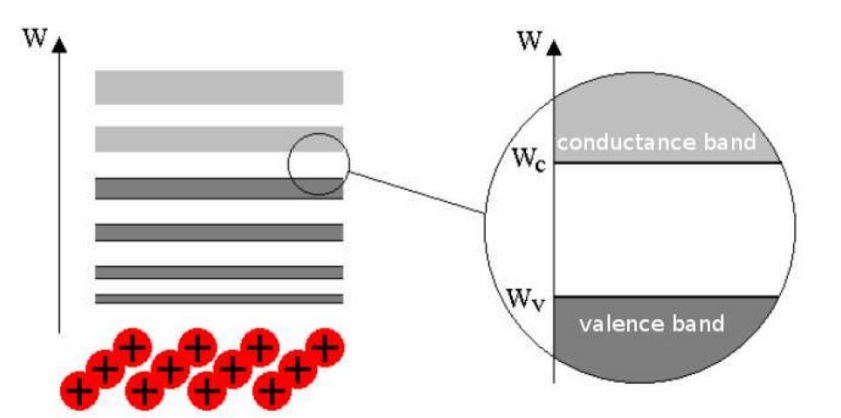


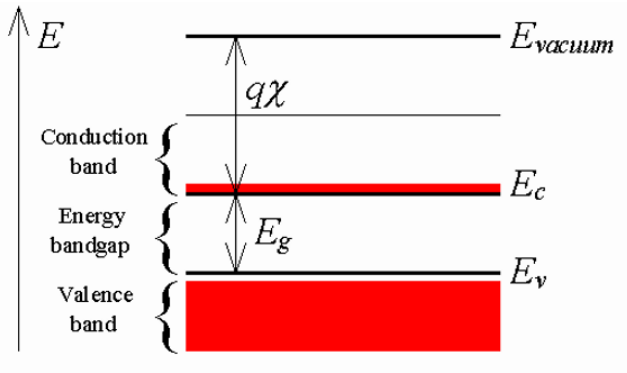
- **Crystalline:** materials in which atoms are placed in a high ordered structure.
- **Poly-crystalline:** These materials consist of small crystalline regions with random orientation called grains, separated by grain boundaries.
- **Amorphous:** materials in which atoms are placed randomly.

The Energy band structure

- An electron's energy is a quantized quantity. When electrons take part in a system, every electron has to be at a different energy level.

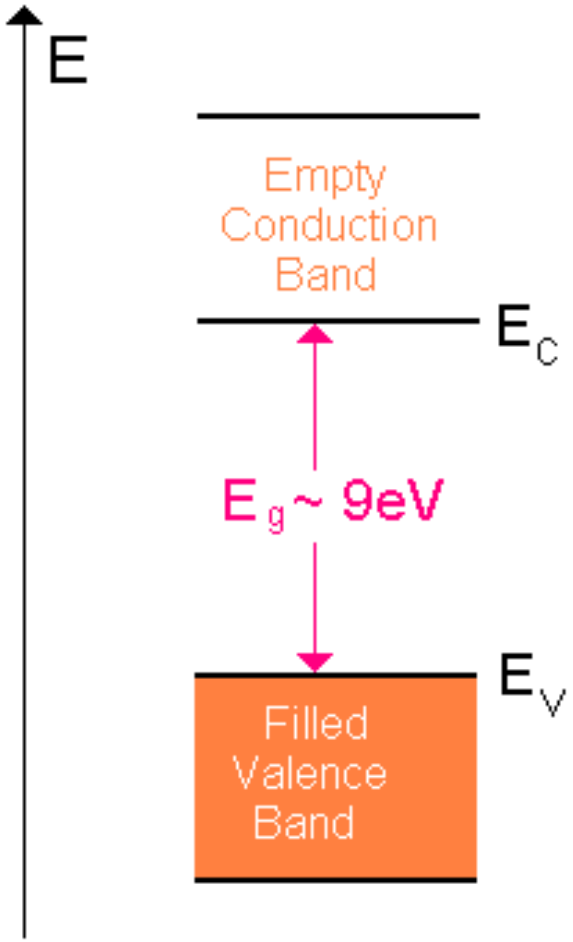
- Complete energy band diagrams are very complex. The energy levels are grouped in bands, separated by energy band gaps.





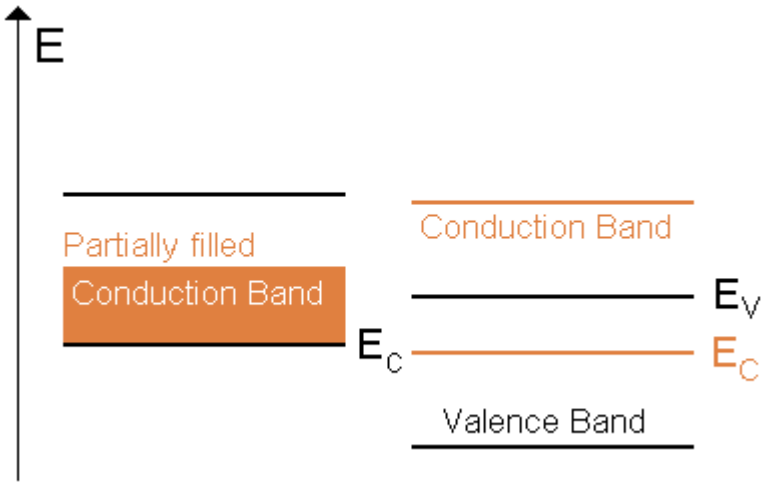
Energy band of Insulator:

- Large bandgap.
- All the energy levels in the valence band are occupied by electrons
- All energy levels in the conduction band are empty.
- Thermal energy or an applied electric field cannot raise the uppermost electron in the valence band to the conduction band.
- It cannot conduct current



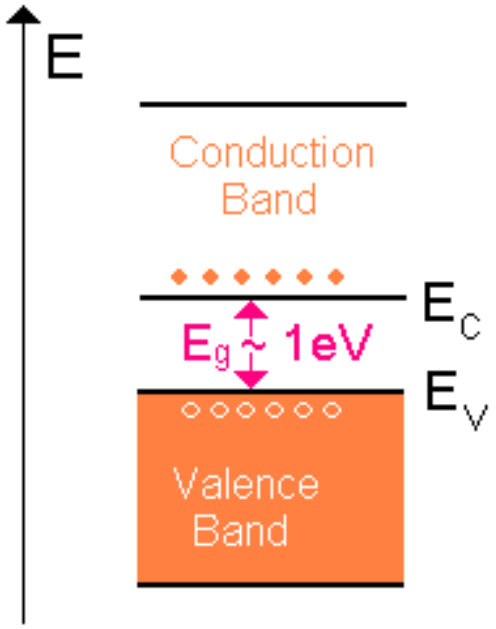
Energy band of Conductors:

- The conduction band overlaps the valence band so that there is no bandgap.
- The conduction band is partially filled.
- The uppermost electrons in the partially filled band or electrons at the top of valence band can move to the next-higher available energy level when they gain kinetic energy.
- They conduct current



Energy band of Semiconductors:

- Bonds between neighboring atoms are only moderately strong
- Some electrons will be able to move from valence band to the conduction band, leaving holes in the valence band.
- When an electric field is applied, electrons and holes will gain kinetic energy and conduct electricity

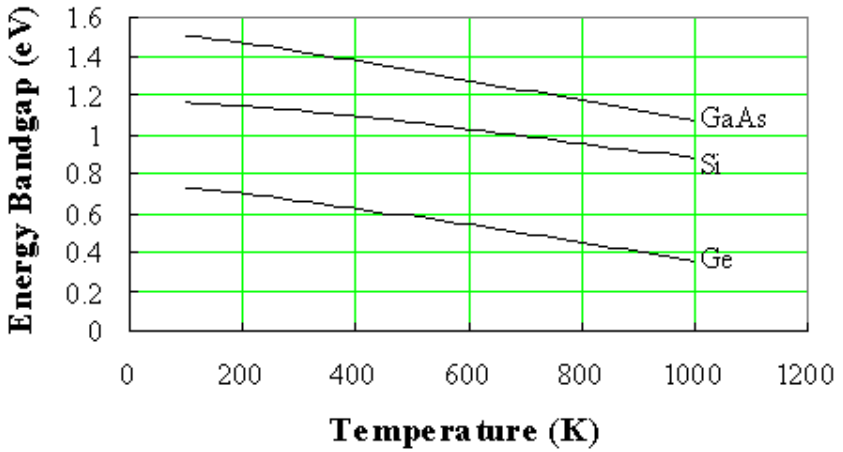


Temperature dependence of the energy bandgap:

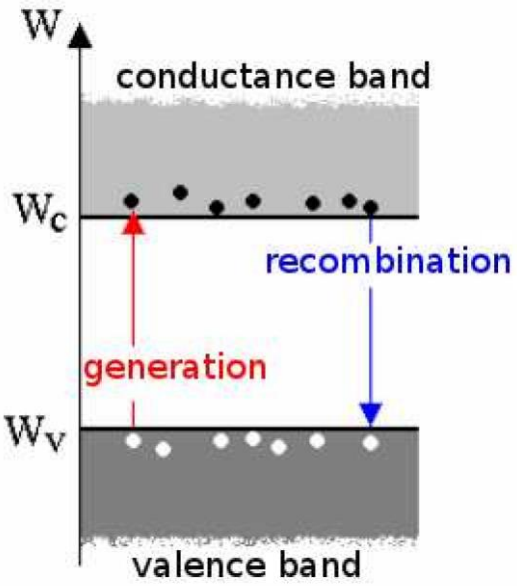
- The energy bandgap of semiconductors tends to decrease as the temperature is increased.
- The variation of bandgaps with temperature can be expressed:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta}$$

	Silicon	GaAs	Germanium
$E_g(0)$ (eV)	1.166	1.519	0.7437
α (meV/K)	0.473	0.541	0.477
β (K)	636	204	235



Charge carriers



- Electrons: at the bottom of the conductance band while the holes at the top of the valence band – a hole is an absence of electron.
- Generation: happens when an electron gets to the conductance band from the valence band.
  - This means that two charge carriers are created: an electron in the conductance band and a hole in the valence band.
- Recombination: the opposite of generation – when an electron falls back to the valence band.

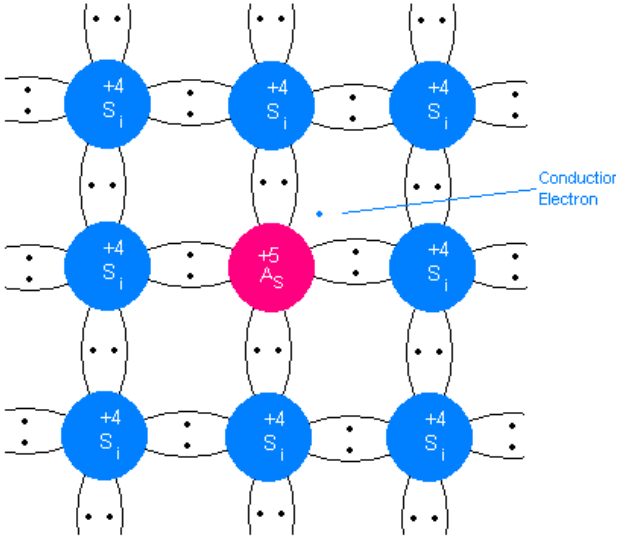
Doping

- A small number of atoms of a different element are injected into the crystal structure. Therefore, dopants are placed in positions where Si atoms are normally located.

- There are two types of doping

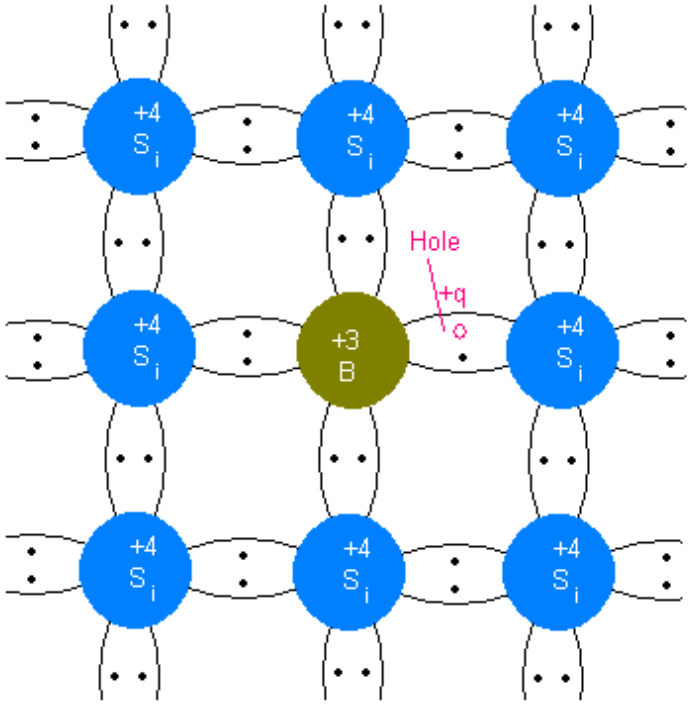
1. n-type doping

  - The generation of free carriers requires not only the presence of impurities, but also that the impurities give off electrons to the conduction band in which case they are called donors.
  - Electrons are the majority charge carriers, **holes** are the minority charge carriers

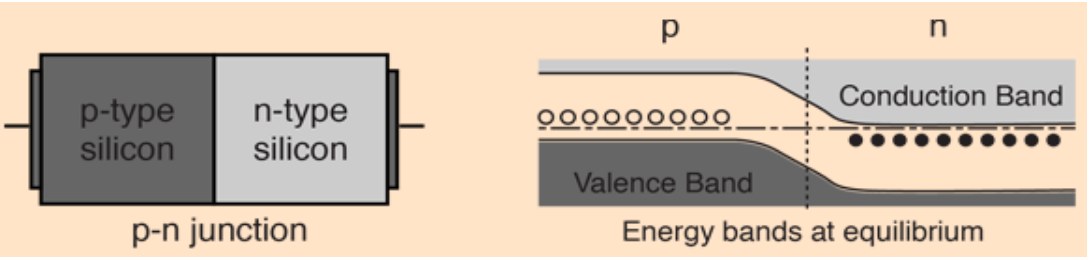


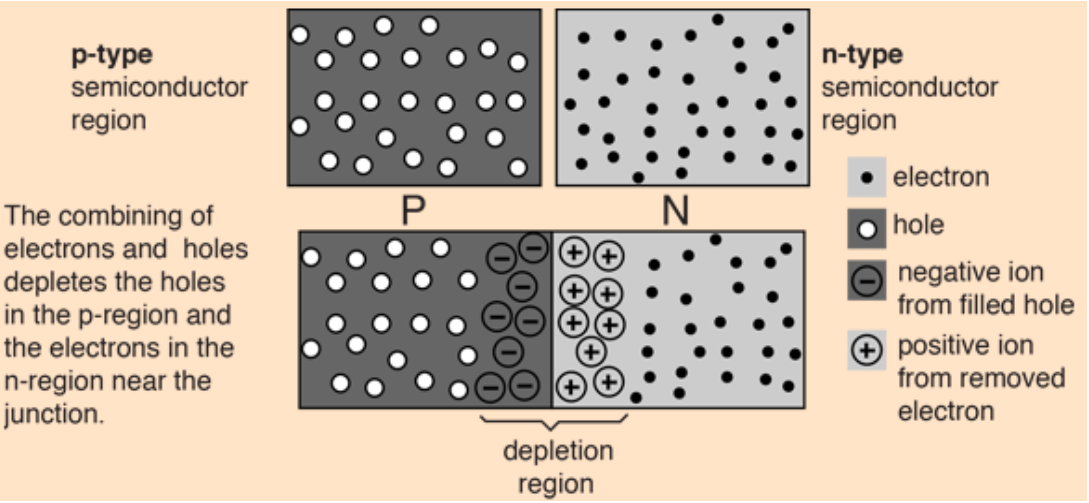
2. p-type doping:

- The impurities give off holes to the valence band, in which case they are called acceptors
- Electrons are the minority charge carriers, holes are the majority charge carriers

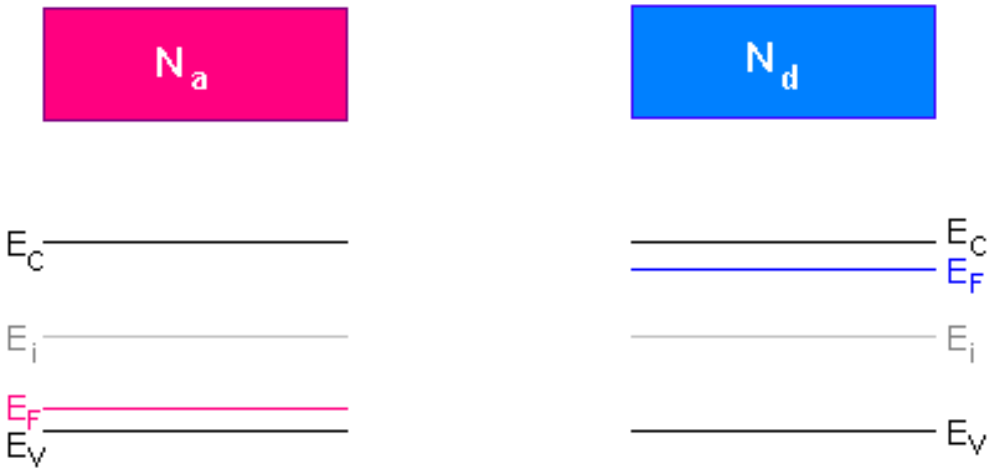


The pn-junction (a semiconductor diode)

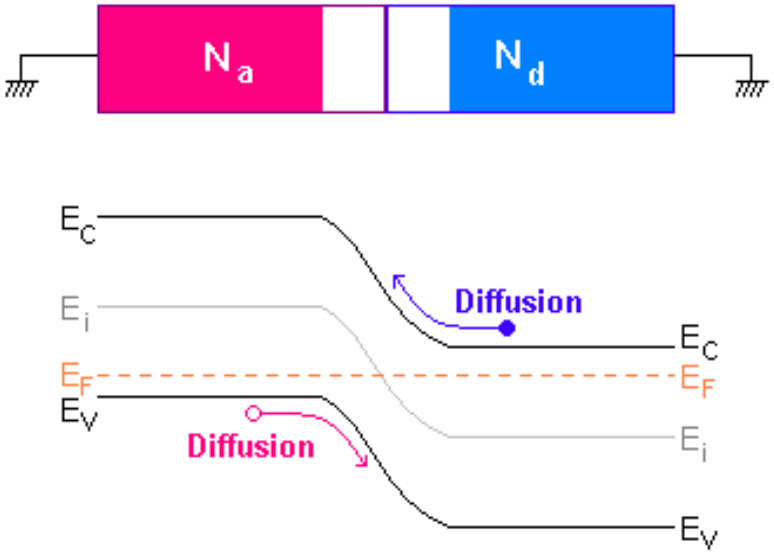




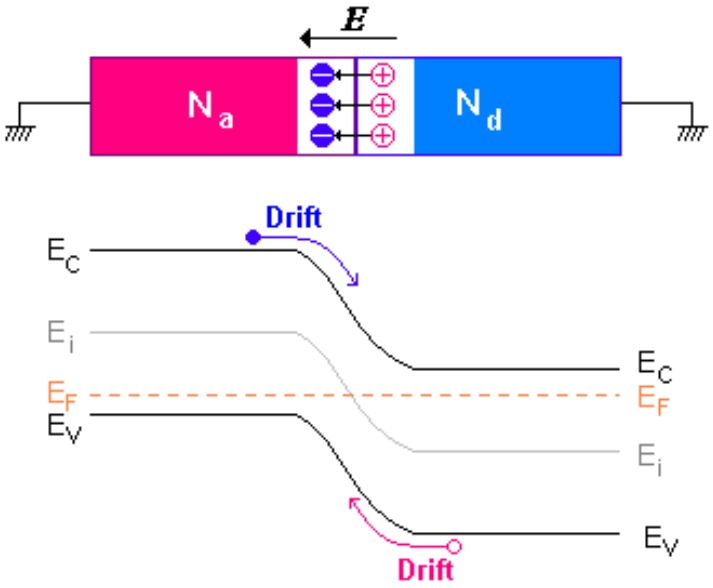
- A p-n junction consists of two semiconductor regions with opposite doping type.
- The p-type semiconductor has an acceptor density N_a.
- The n-type has a donor density N_d.



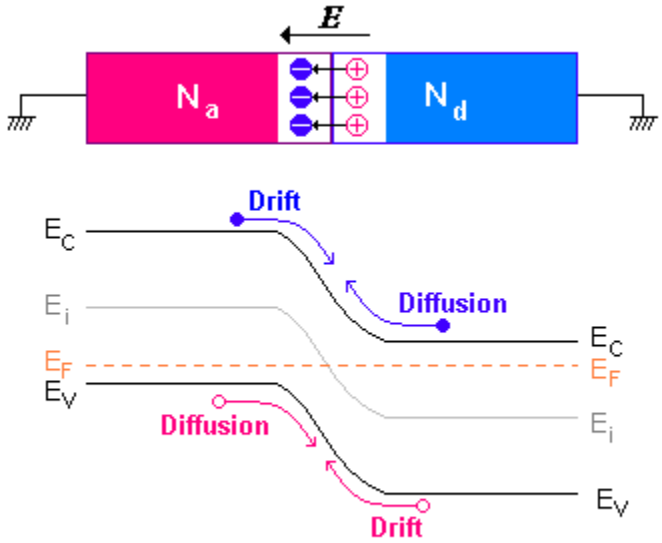
- The large carrier concentration gradients at the junction cause **carrier diffusion**:
  - Holes from the p-side diffuse into the n-side
  - Electrons from the n-side diffuse into the p-side



- **Negative space charge** near the p-side of the junction: As holes continue to leave the p-side, some of the negative acceptor ions (N_a^-) near the junction are left uncompensated.
- A **positive space charge** near the n-side: some of the positive donor ions (N_d^+) near the junction are left uncompensated as the electrons leave the n-side.

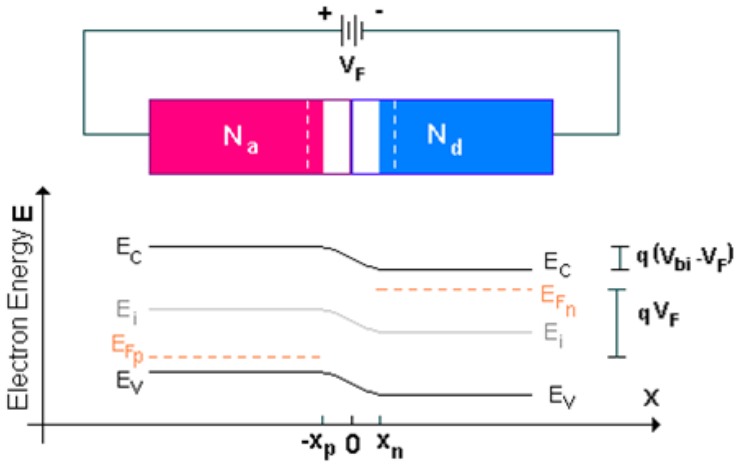


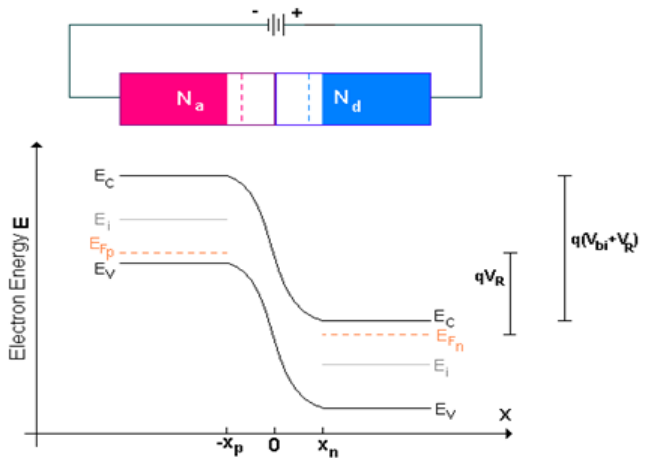
- At thermal equilibrium (steady-state condition) without external excitations, the net current flow across the junction is zero.
- The Fermi level must be constant (condition of zero net electron and hole current)



- Forward-biased p-n junction:
  - **positive voltage** "V_F" applied to the p-side.
  - The depletion width decrease with the increasing of the applied voltage:

- **Reverse-biased** p-n junction:
  - positive voltage "**V_R**" applied to the **n-side.**
  - The depletion width increases with the increasing of the applied voltage:



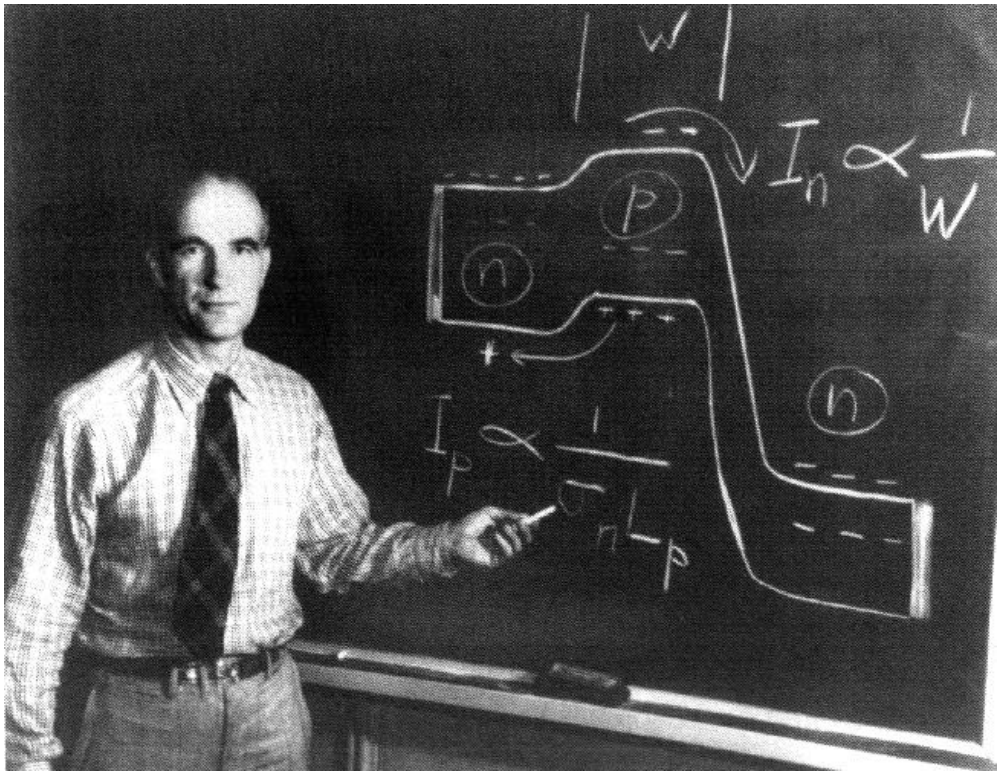


The Transistor Era

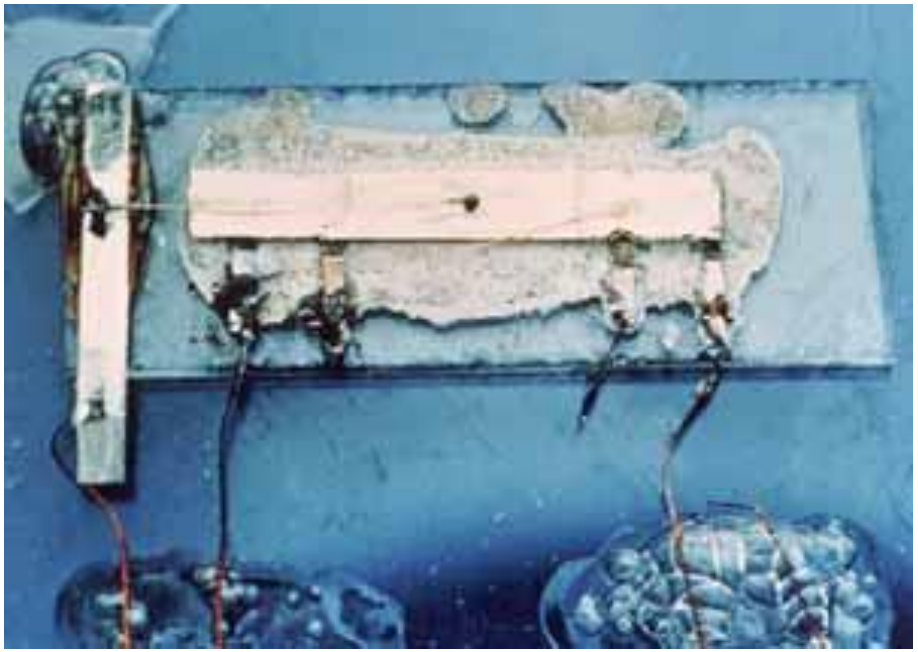
- 1947 **- John Bardeen, Walter Brattain, and William Shockley** invented the first Transistor: the Point-Contact Transistor, at Bell Laboratories.

- 1948 - **Shockley** invents junction transistor:

  Three layers of semiconductors all piled together. The junction Transistor involved current flowing directly through the chunks of semiconductors, not along the surface.



- 1954 - First Transistor Radio
- 1954 - First fully transistorized computer
- 1956 - Nobel Prize Awarded to Shockley, Brattain & Bardeen
- 1958 – **J. Kilby** invents integrated circuit at the Texas Instruments Lab



History

- 1906 – Semiconductors used to detect radio signals
- 1925 – FET concept patent by J. Lilienfeld1941 – Z3 by Konrad Zuse – first computer
- 1946 – ENIAC – first electronic computer
- 1947 – Transistor “Invented”
  - AT&T ignores LilienfeldBardeen,
  - Brattain and Schockley, AT&T, Nobel Prize in 1956
- 1958 – Integrated Circuit
  - Kilby & Noyce (died 1990)
  - Kilby - Noble Prize in 2000
- 1960- MOSFET manufactured and patented
- 1963- CMOS logic invented
  - Resistors replaced by transistorsMicro transductors ‘08, CMOS Basics

https://youtu.be/7ukDKVHnac4

Microelectronics& Integrated Circuits IC's

- Microelectronics is a subfield of electronics, and it relates to the study and manufacturing of very small electronic designs and components
  - These devices are typically made from semiconductor materials.
- An integrated circuit (IC), sometimes called a chip or microchip, is a semiconductor wafer on which thousands or millions of tiny resistors, capacitors, and transistors are fabricated.
  - An IC can function as an amplifier, oscillator, timer, counter, computer memory, or microprocessor.

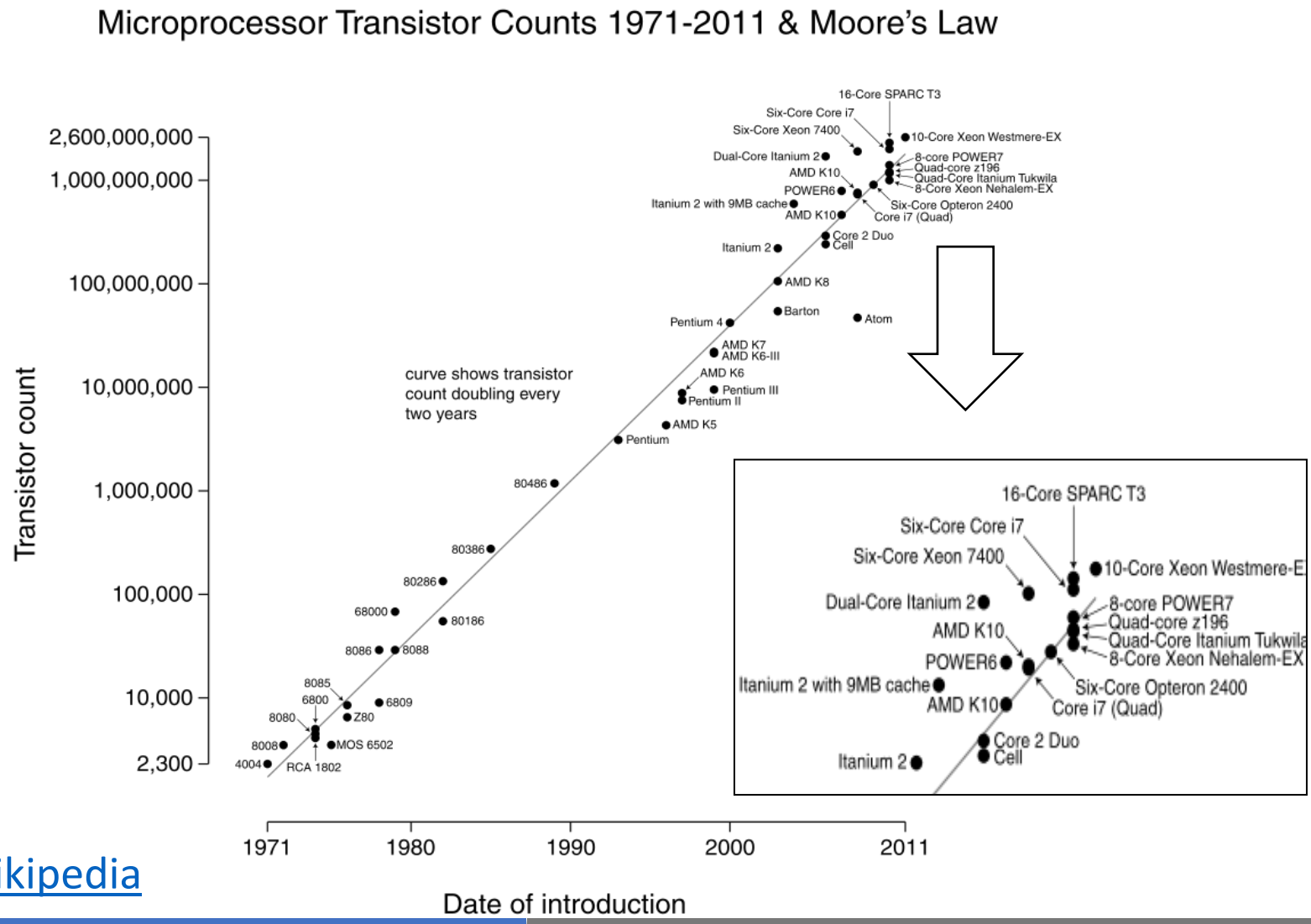
Moore's law

- Gordon Moore made a prediction in 1965, that the number of transistors integrated on one chip would double every 18-24 month (exponential growth).

- The 1 million transistors per chip barrier was broken through in the 80's:

  - 1971: 2300 transistors, clock frequency: 1 MHz (Intel 4004)
  - 2001: 42 million transistors, clock frequency: 2 GHz (Intel P4) – 2001
  - 2016: 7.2 billion transistors, 22-core Xeon Broadwell-E5
    - 2.2GHz (3.6GHz in turbo mode), 55MB smart cache, 456mm^2
  - FPGA: 30 billion transistors, Stratix 10 10GX5500/10SX5500

Evolution of Microprocessors



- Source: [wikipedia]

- Integrated circuits can be classified into two groups based on the type of transistors they contain.

1. Bipolar integrated circuits contain bipolar junction transistors as their principle elements.
2. Metal-oxide-semiconductor (MOS) integrated circuits contain MOS transistors as their principle elements.

- Integrated circuits are also categorized according to the number of transistors or other active circuit devices they contain.

1. A small-scale integration (SSI) IC contains fewer than 10 transistors.
2. A medium-scale integration (MSI) IC contains from 10 to 100 transistors.
3. A large-scale integration (LSI) IC contains from 100 to 1,000 transistors.
4. A very-large-scale integration (VLSI) contains more than 1,000 transistors.

- All ICs now employ VLSI, and these distinctions are only of historical importance.

- Some integrated circuits are analog devices; an operational amplifier is an example.

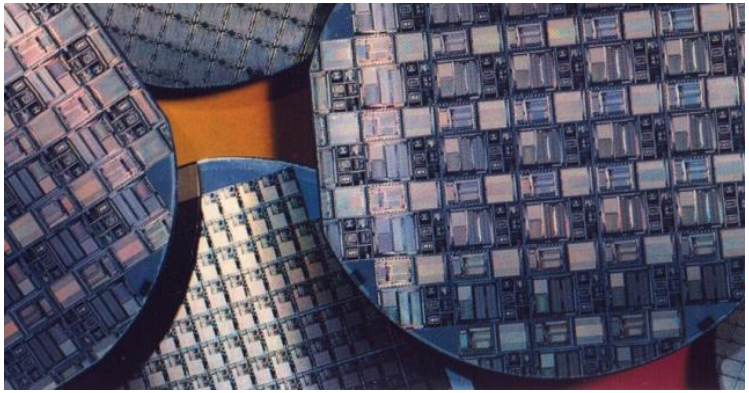
- Other ICs, such as the microprocessors used in computers, are digital devices.

- Some hybrid integrated circuits contain both analog and digital circuitry; a bilateral switch, which switches analog signals by means of a digital control signal is an example of a hybrid IC.

Planar technology

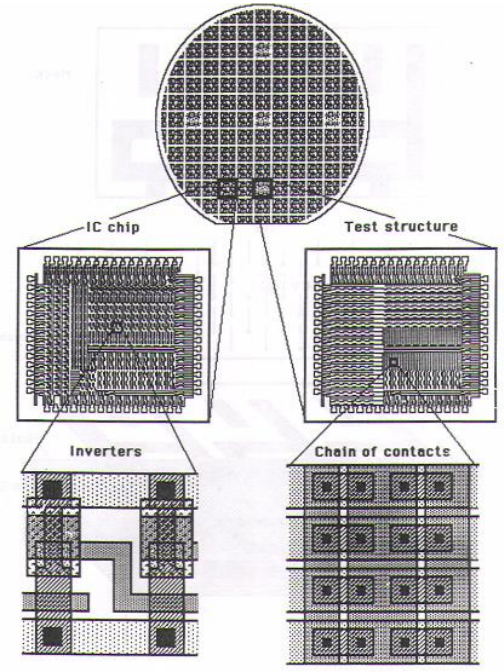
- Very large scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining millions of MOS transistors onto a single chip.

- Most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI enables IC designers to add all of these into one chip.



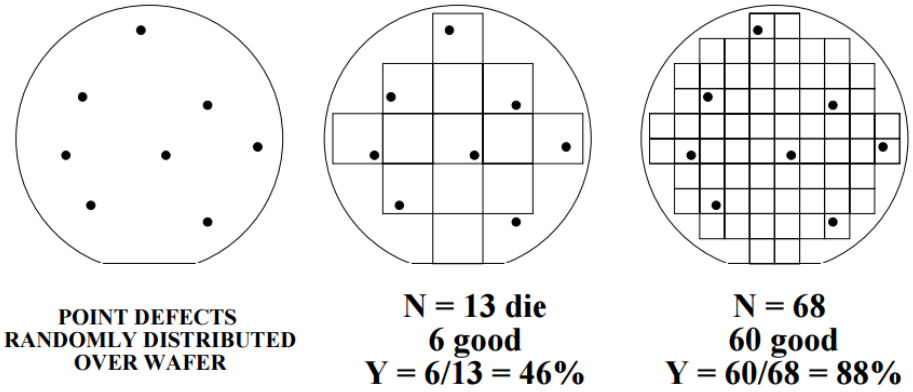
- The word planar implies that the devices are fabricated on the surface of the silicon wafer in a 2D structure.

- The basis is a silicon ingot made up of monocrystalline silicon. The ingot is sliced into wafers. A wafer can contain thousands of ICs that are manufactured at the same time.



Trends in Integrated Circuit Technology

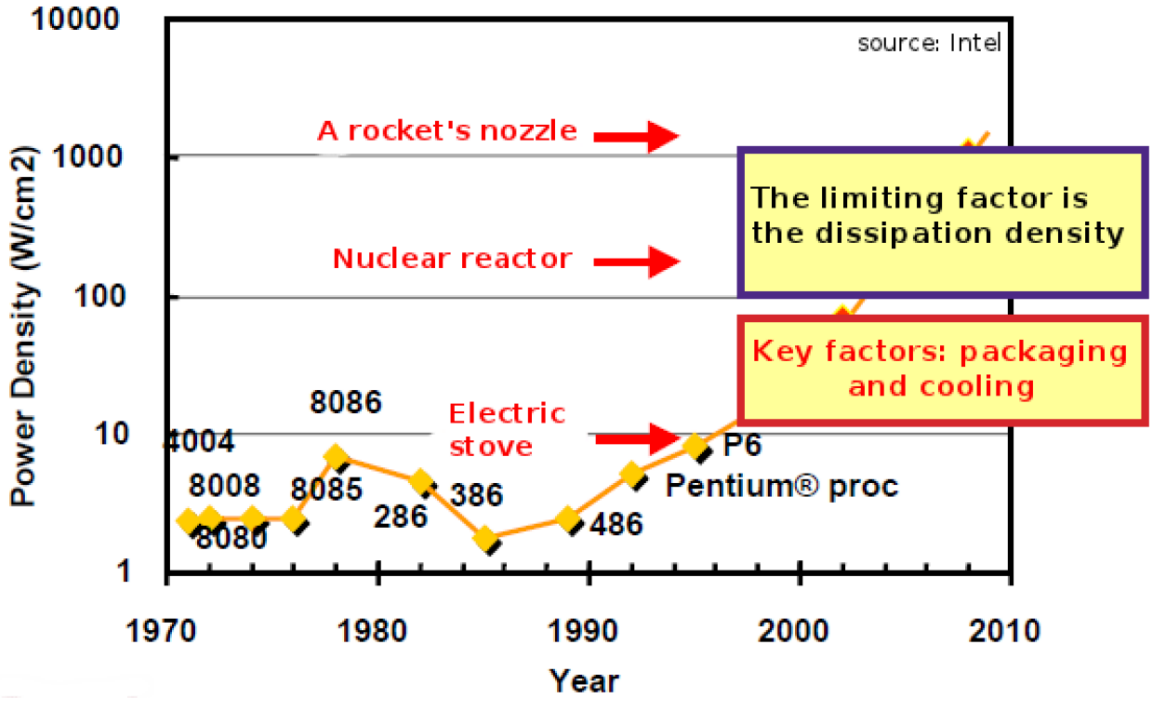
- The number of components can be increased in two ways
  - Increasing the size of the chip.
    - But it ends up with more failures per wafer (lower yield) due to randomly distributed defects on wafers.
    - Optimal chip area is about 500mm^2



  - If we can decrease every physical size by the factor of 2, we can produce 4 times more components. This is called scaling

- Effects of scaling
  - Delay can be decreased (clock frequency can be increased)
  - Power consumption of logic gates decreases
  - Power dissipation density increases!

- Dissipation density



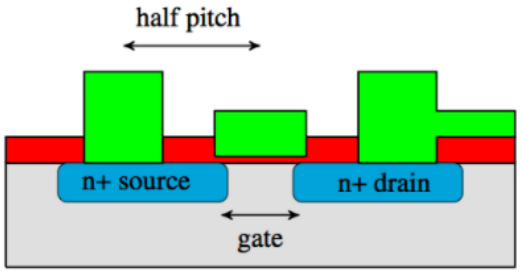
- If scaling continues at present pace, high speed processors would have power density of nuclear reactor by 2005, a rocket nozzle by 2010 and a surface of the sun by 2015 !

- Why Power Matters

1. Packaging costs.
2. Power supply rail design.
3. Chip and system cooling costs.
4. Noise immunity and system reliability.
5. Battery Life (in portable systems).

- This reason led us to design multi-core processors
  - 2004: Power Wall, which has limited the frequency to 3-4GHz

- A specific semiconductor process has specific rules on the minimum size and spacing for features on each layer of the chip.



- The half pitch of the first metallization layer is the defining feature for chips. The gate width represents the smallest feature.

- The shrinking trend of feature size led to the classification of different generations of ICs, giving rise to new design methods from the early small-scale integration (SSI) to the more complex ultra-large-scale integration (ULSI) and three-dimensional integrated circuit (3D-IC)

Technology node

- The technology node (also process node, process technology) refers to a specific semiconductor manufacturing process and its design rules.
- Historically, the process node name referred to a number of different features of a transistor including the gate length as well as half-pitch.
- Generally, the smaller the technology node means the smaller the feature size, producing smaller transistors which are both faster and more power-efficient.

MOSFET scaling (process nodes)
10 µm – 1971
6 µm – 1974
3 µm – 1977
1.5 µm – 1981
1 µm – 1984
800 nm – 1987
600 nm – 1990
350 nm – 1993
250 nm – 1996
180 nm – 1999
130 nm – 2001
90 nm – 2003
65 nm – 2005
45 nm – 2007
32 nm – 2009
22 nm – 2012
14 nm – 2014
10 nm – 2016
7 nm – 2018
5 nm – 2020
Future3 nm ~ 2022
2 nm ~ 2024

- The ITRS roadmaps always contain the latest predictions and directions of the development.
- They are created by the leaders of the industry.
- Forecast from 2015 can be found here.

YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	FinFET FDSOI	FinFET FDSOI	FinFET LGAA	FinFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D

- We will revisit these abbreviations (FinFET, FDSOI, LGAA, VGAA) later

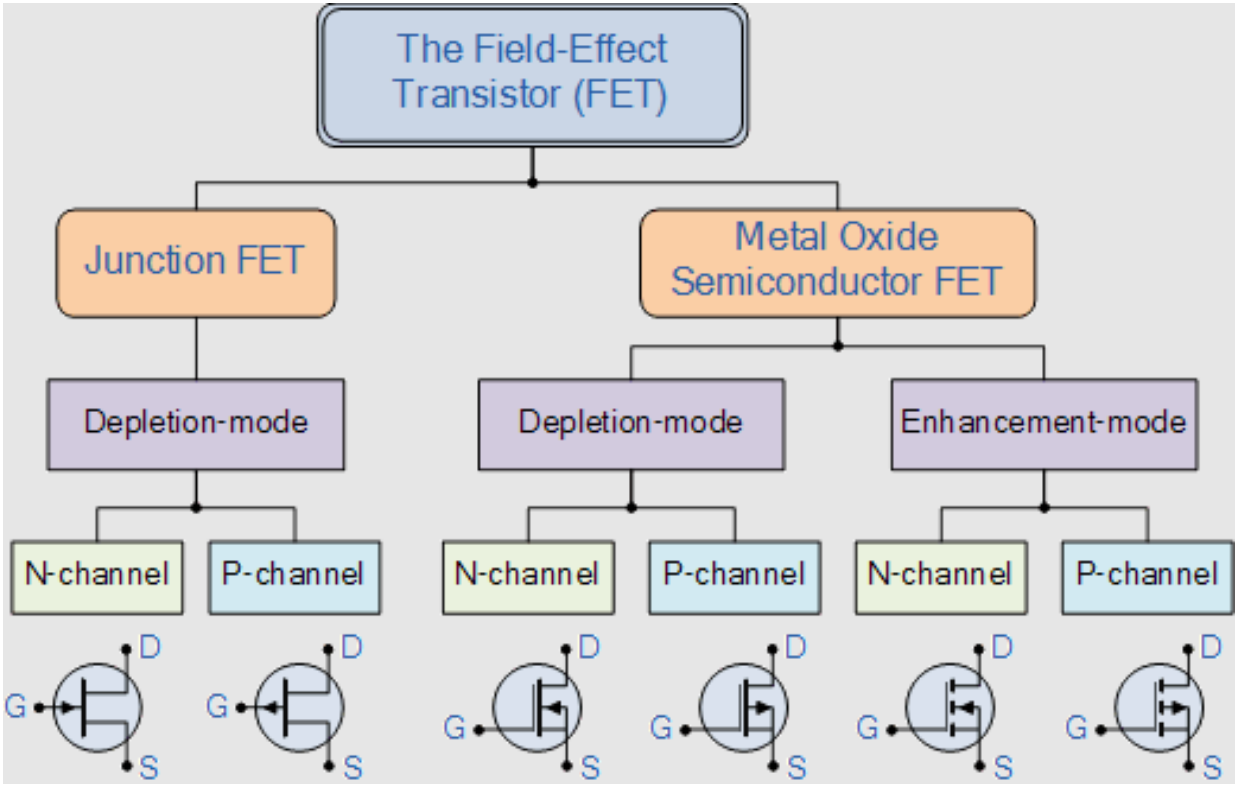
Budapest University of Technology and Economic
Department of Electron Devices

Circuit Environment

Lecture 2

- Field Effect Transistors Classification
- MOSFET Transistors
- The Operation of MOSFET Transistor
- Fabrication Process Technologies

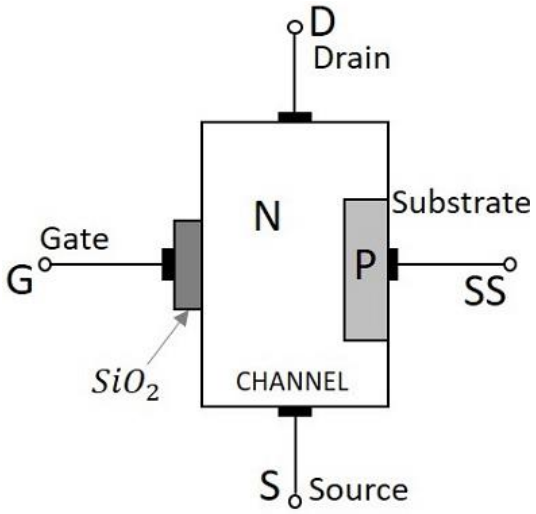
Field Effect Transistors classification



- MOSFET differs from a JFET in that it has a “Metal Oxide” Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide.

MOSFET Transistors

- MOS: Metal-Oxide-Semiconductor
  - MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available.
  - The Substrate terminal is not normally used as either an input or an output connection but instead it is used for grounding the substrate.



- The MOSFET acts like a voltage controlled resistor as the current flowing through the main channel between the Drain and Source is proportional to the input voltage.

- The MOSFETs are available in two basic forms:

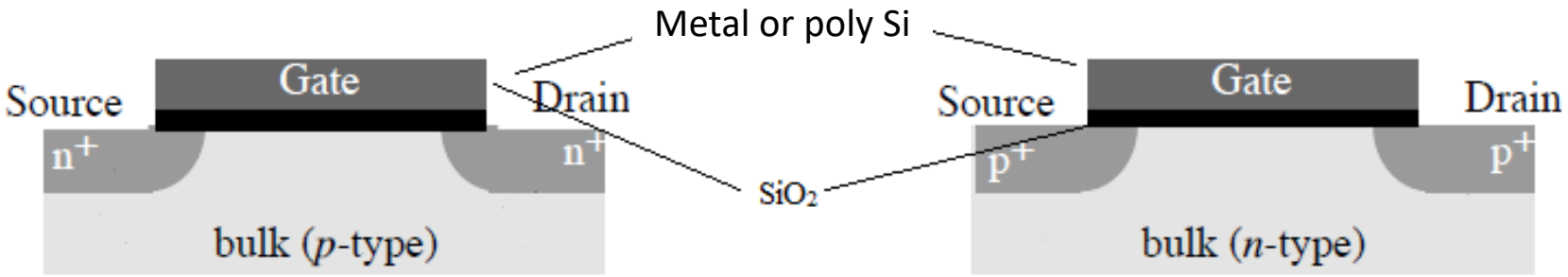
  - Depletion Type – the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device “OFF”. The depletion mode MOSFET is equivalent to a “Normally Closed” switch.

  - Enhancement Type – the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device “ON”. The enhancement mode MOSFET is equivalent to a “Normally Open” switch.

- Both the Depletion and Enhancement type MOSFETs use an electrical field produced by a gate voltage to alter the flow of charge carriers, electrons for n-channel or holes for P-channel, through the semiconductive drain-source channel.

- There are two types of MOS transistors.

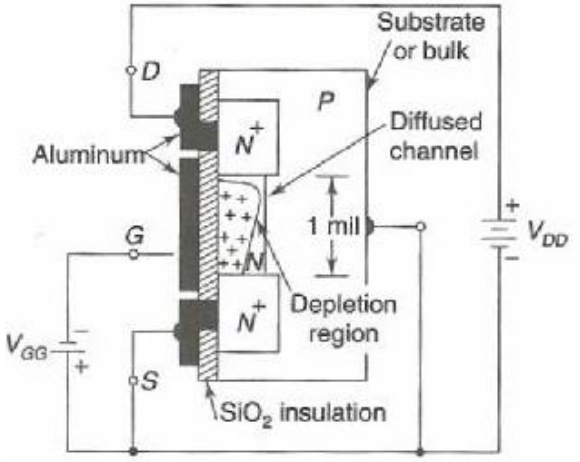
  - nMOS: the bulk is p-type silicon (the inversion channel is n-type)
  - pMOS: the bulk is n-type silicon (the inversion channel is p-type)



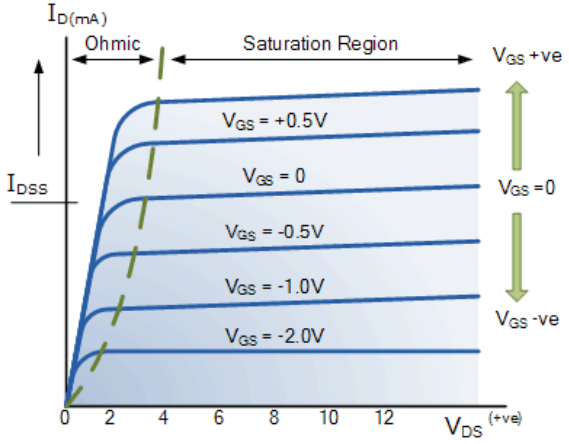
The Operation of MOSFET Transistor

- Depletion-mode MOSFET
  - The drain-source channel is conductive with the electrons and holes already present within the n-type or p-type channel. This doping of the channel produces a conducting path of low resistance between the drain and source with zero Gate bias.
  - It normally switched “ON” (conducting) without the application of a gate bias voltage. That is the channel conducts when $V_{GS} = 0$, making it a “normally-closed” device.
  - For the n-channel depletion MOS transistor, a negative gate-source voltage, $-V_{GS}$ will deplete the conductive channel of its free electrons switching the transistor “OFF”.

- Likewise for a p-channel depletion MOS transistor a positive gate-source voltage, + V_{GS} will deplete the channel of its free holes turning it “OFF”.



- The I-V Characteristic of n-channel depletion MOS transistor is:

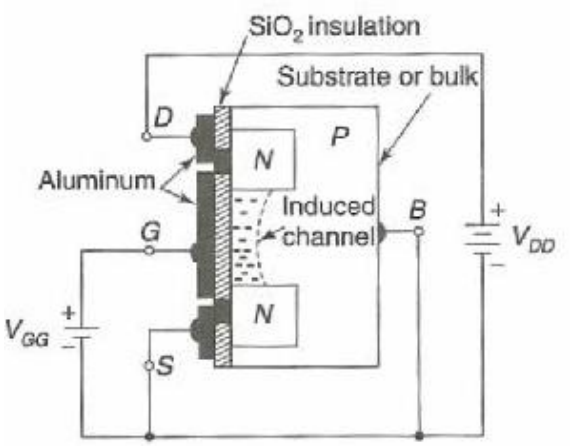


- Enhancement-mode MOSFET

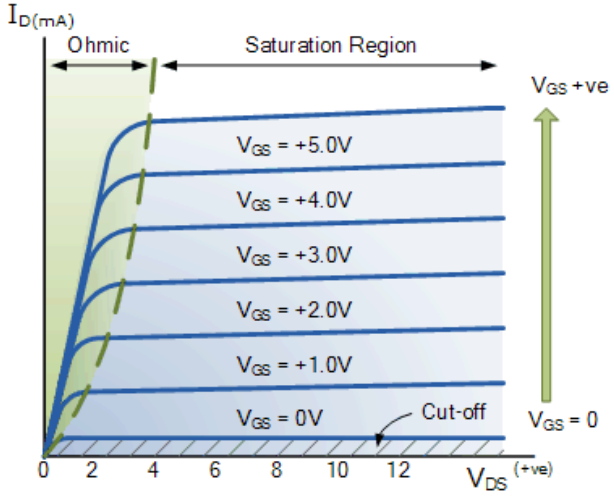
  - Here the conducting channel is lightly doped or even undoped making it non-conductive. This results in the device being normally “OFF” (non-conducting) when the gate bias voltage, V_{GS} is equal to zero.

  - For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage (V_{GS}) is applied to the gate terminal greater than the threshold voltage (V_{TH}) level.

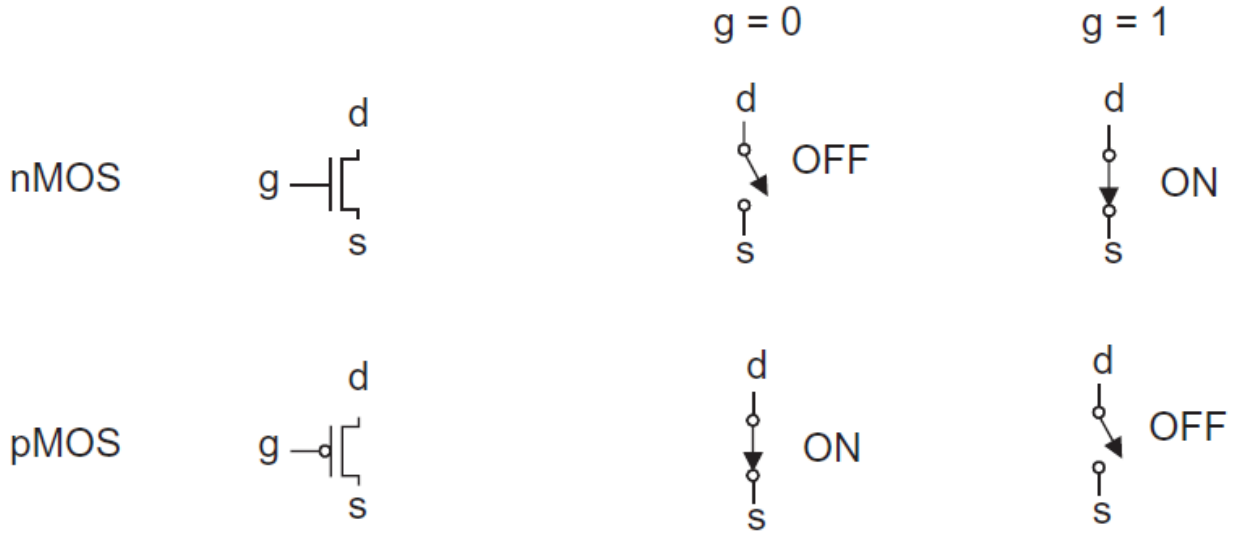
  - The application of a positive (+ve) gate voltage to a n-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing the thickness of the channel allowing more current to flow.



- The reverse is true for the p-channel enhancement MOS transistor. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it “ON”.
- The I-V Characteristic of n-channel enhancement MOS transistor is:



- MOS transistors as switch



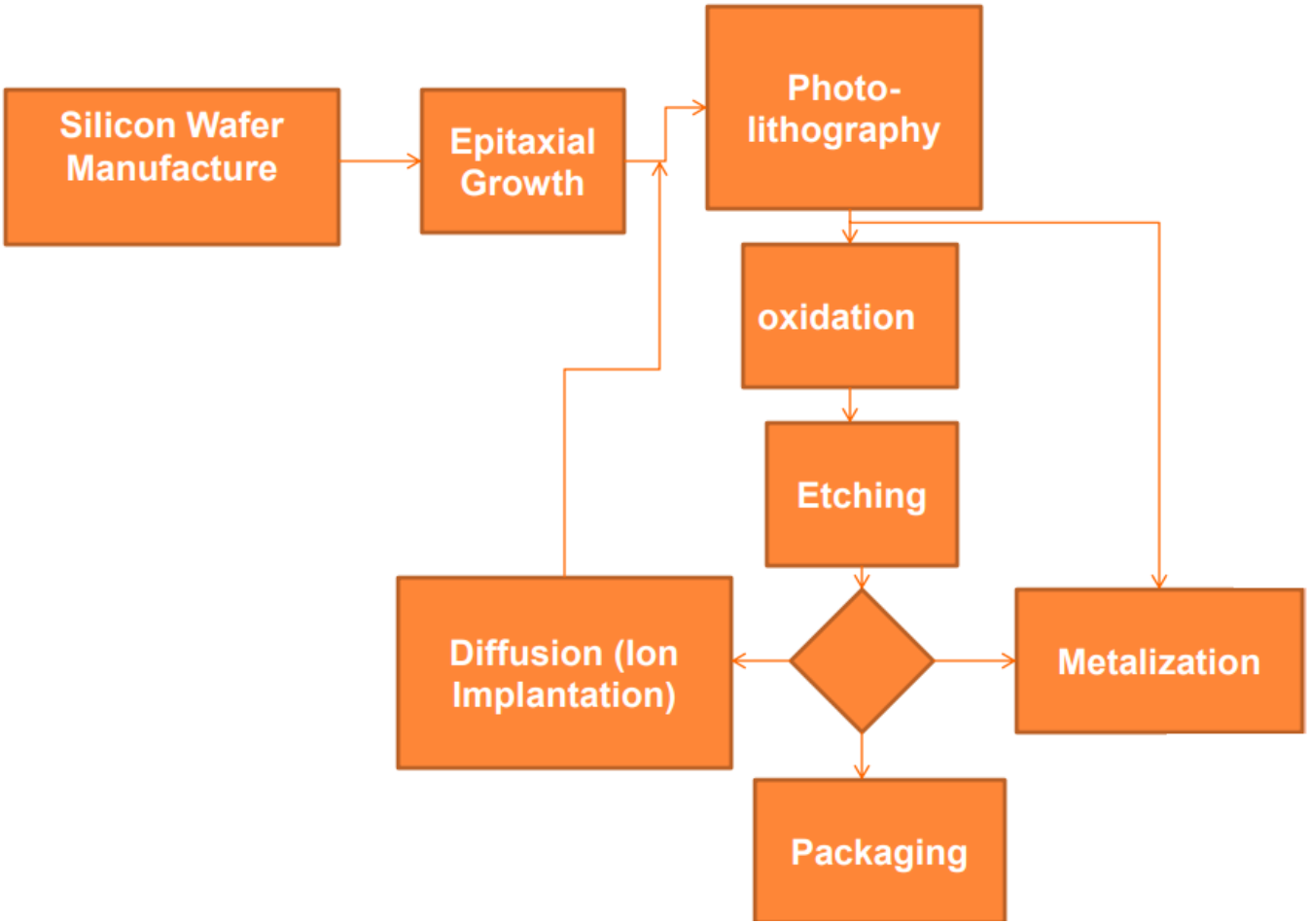
  - nMOS
    - In case of logical 0: open switch (does not conduct current)
    - In case of logical 1: closed switch (conducts current)
  - pMOS
    - logical 0: conducts current,
    - logical 1: does not conduct current

- The symbol of pMOS transistor has a circle at the gate terminal

Complementary Metal Oxide Semiconductor (CMOS)

- Complementary MOS
  - They consist of two types of MOSFETs: n-type and p-type
  - Nowadays, logic circuits are CMOS.
- We have two complementary transistors:
  - One conducts when the input logic level is high
  - Other conducts when the input logic level is low
- We can create
  - Inverters
  - Basic logic gates (and, or, etc.)
  - Complex logic gates

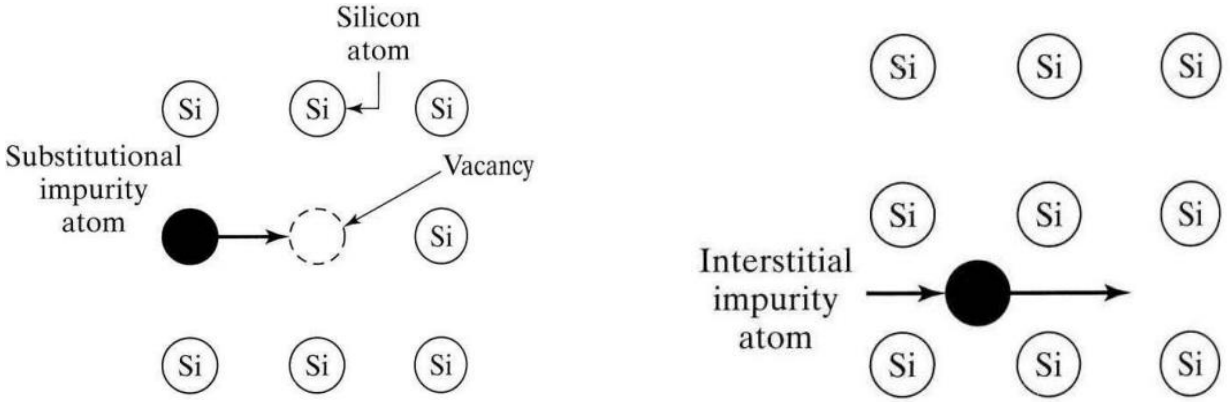
Fabrication Process Technologies



Impurity Doping

- Two methods for introducing impurities into Si to control the majority-carrier type and resistivity of layers.

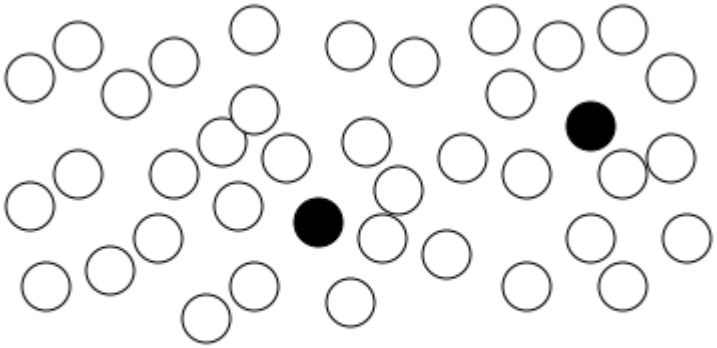
  - Diffusion: dopant atoms move from the surface into Si by thermal means via substitutional or interstitial diffusion mechanisms.



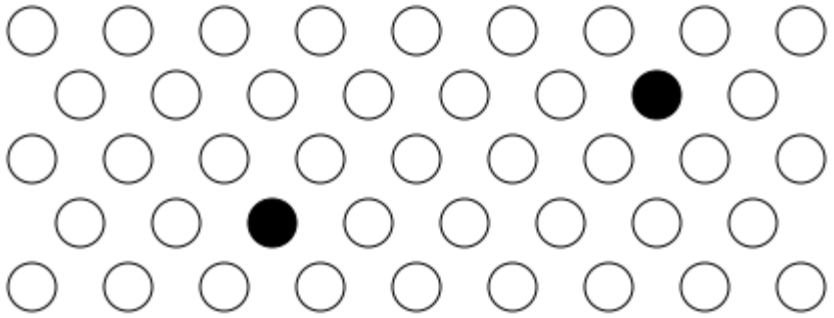
  - Ion implantation: dopant atoms are forcefully added into Si in the form of energetic ion beam injection. Thermal Annealing is required.

What Annealing

- Is the process of heating a metal or alloy to an appropriate temperature for a certain period of time and then slowly cooling (generally with the furnace cooling). The annealing can
    - Decrease the number of lattice imperfection/distortion (e.g. after ion implantation, after oxide growth).
    - Activate dopant atoms after implantation (atoms diffuse into vacancies from substitutional positions).
    - Decrease residual stress in deposited layers and improve adhesion.



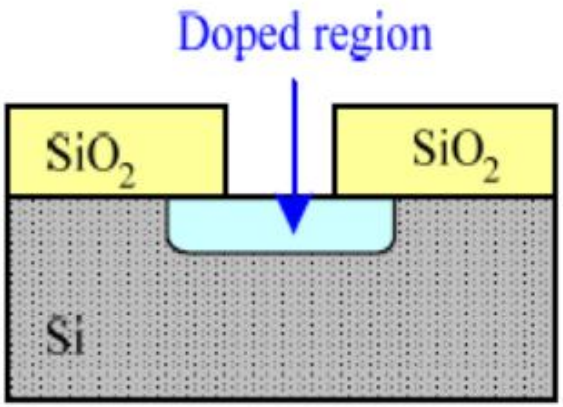
Before Annealing

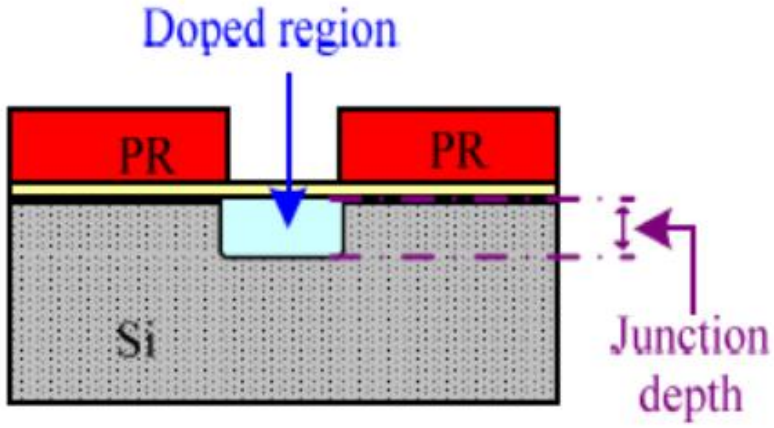


After Annealing

Doping Techniques Comparison

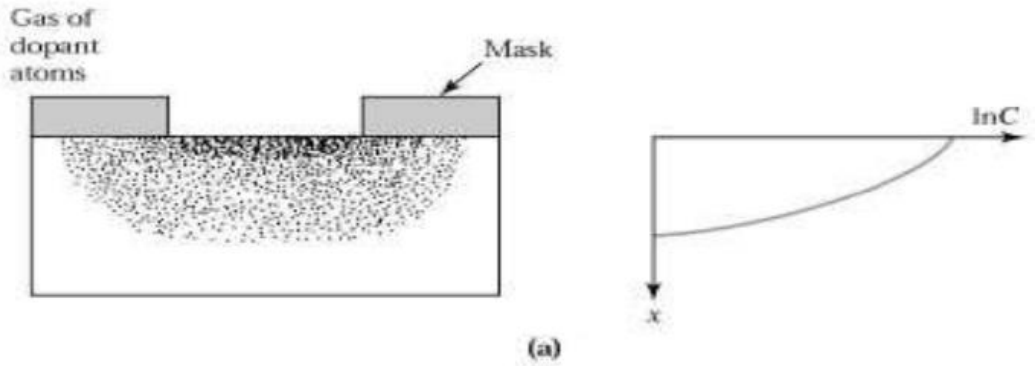
Diffusion	Ion Implantation
•High temperature, hard mask (SiO_2)	•Low temperature, PR mask
•Isotropic dopant profile	•Anisotropic dopant profile
•Cannot independently control the dopant concentration, junction depth	•Can independently control the dopant concentration, junction depth



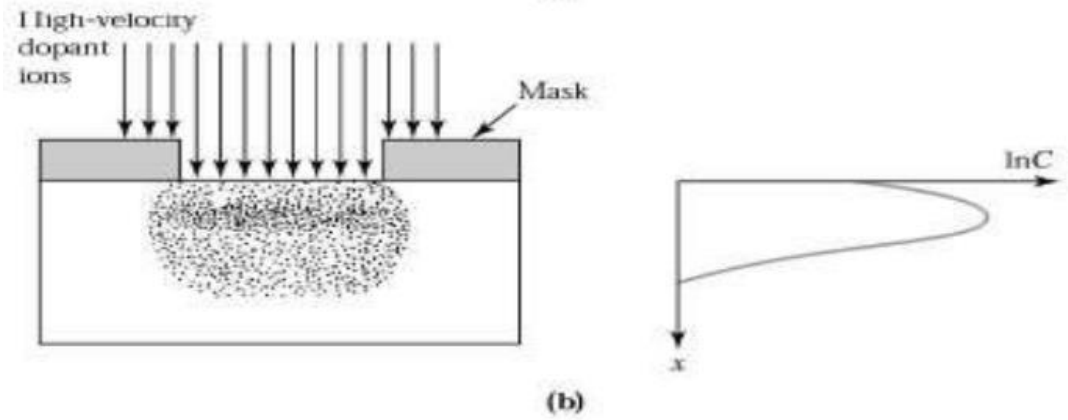


Doping Profile

Diffusion

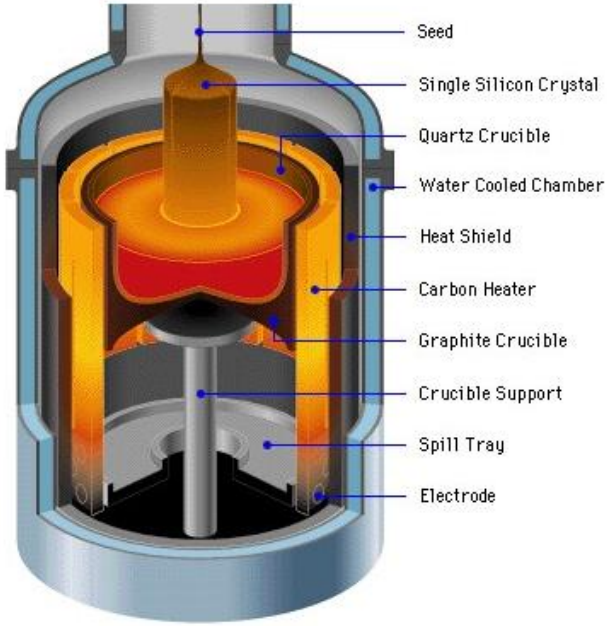


Ion Implantation



Wafer growth – Czochralski Method (Cz)

- The Cz process is the most common for large wafer diameter production.
- The puller consists of three main components:



1. A furnace, which includes a fused-silica crucible, a graphite susceptor, a rotation mechanism (clockwise), a heating element, and a power supply.
2. A crystal-pulling mechanism, which includes a seed holder and a rotation mechanism (counter-Clockwise.
3. An ambient control, which includes a gas source, a flow control and an exhaust system.

- Pull rate, melt temperature and rotation rate are all important control parameters.

Layer Growth and Deposition

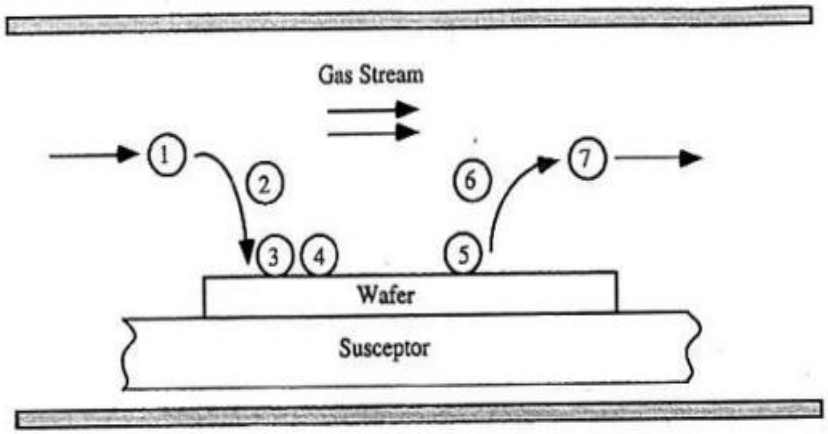
- Chemical Vapour Deposition (CVD) is a chemical process used to produce high purity, high performance solid materials.

- In a typical CVD process, the substrate is exposed to one or more volatile precursors which react and decompose on the substrate surface to produce the desired deposit.

- There are other methods of layer growth and deposition as Physical vapour deposition (PVD), electroless plating, electro plating, Screen printing and Inkjet printing.

- The Steps Involved in CVD

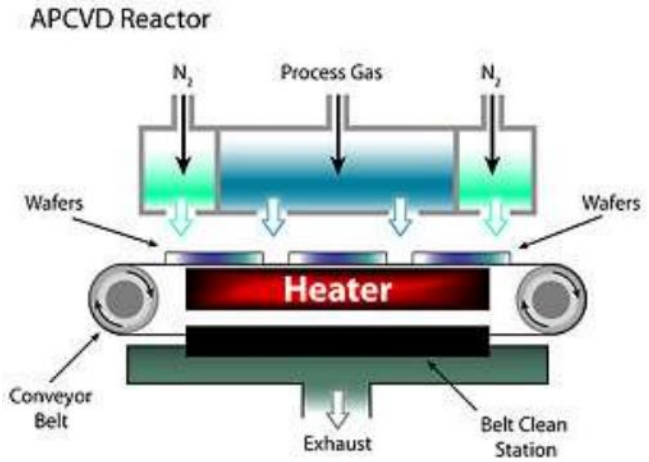
1. Transport of reactants by forced convection to the deposition region.
2. Transport of reactants by diffusion from the main gas stream to the wafer surface.
3. Adsorption of reactants on the wafer surface.
4. Surface processes, including chemical decomposition or reaction, surface migration, site incorporation, and other surface reactions.
5. Desorption of by-products from the surface.
6. Transport of by-products by diffusion back to the main gas stream.
7. Transport of by-products by forced convection away from the deposition region.



Types of CVD

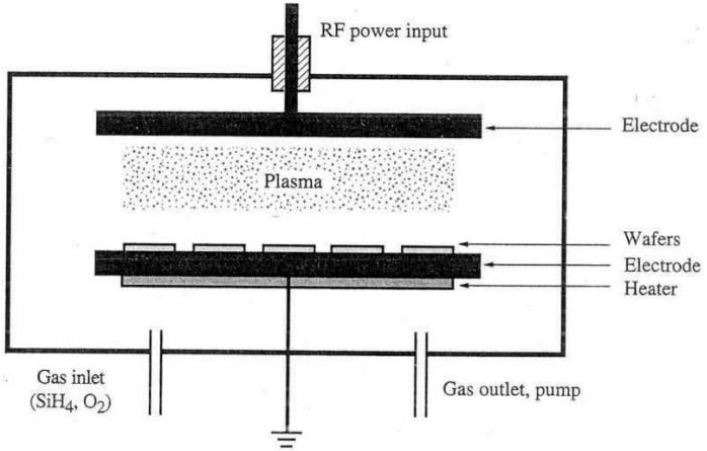
- CVD's are classified into two types on the basis of Operating Pressure.

1. Atmospheric Pressure CVD- APCVD
   - HIGH TEMPERATURE process is used to deposit Silicon and compound films or hard metallurgical coatings like Titanium Carbide and Titanium Nitride.
   - LOW TEMPERATURE process is used to deposit many insulating film layers such as Silicon dioxide for effective deposition.



2. Low Pressure CVD.

- Plasma Enhanced CVD (PECVD).
  - PECVD is a process used to deposit thin films from a gas state (vapor) to a solid state on a substrate.
  - Chemical reactions are involved in the process, which occur after creation of a plasma of the reacting gases.
  - The helping hand of the Plasma helps in increasing the film quality at low temperature and pressure.



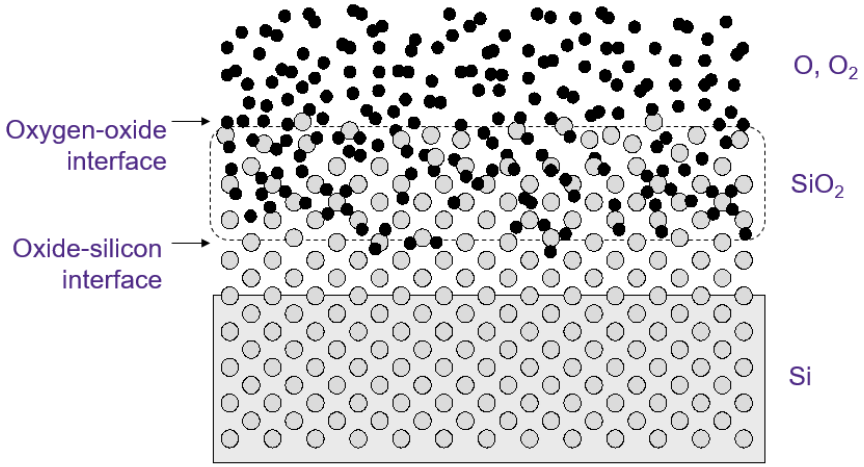
- Photochemical Vapour Deposition.
  - Al thin films are deposited via photochemical vapour deposition on catalytic layers of Ti using dimethyl aluminum hydride.
  - Deposition is carried out at low gas pressures to induce a surface reaction.

- Thermal CVD
  - In thermal CVD process, temperatures as high as 2000 degree Celsius is needed to deposit the compounds.
  - There are two basic types of reactors for thermal CVD.
    1. Hot wall reactor
    2. Cold wall reactor

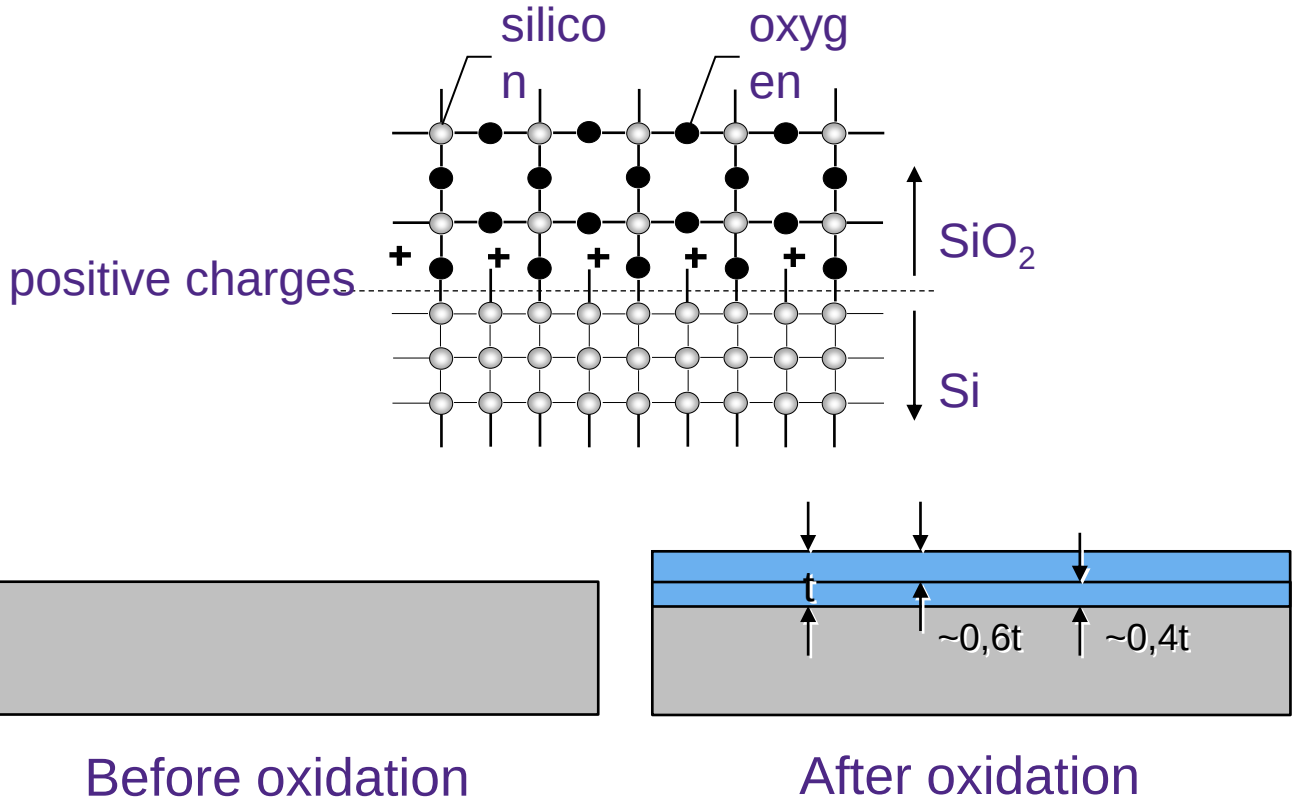
Oxidation

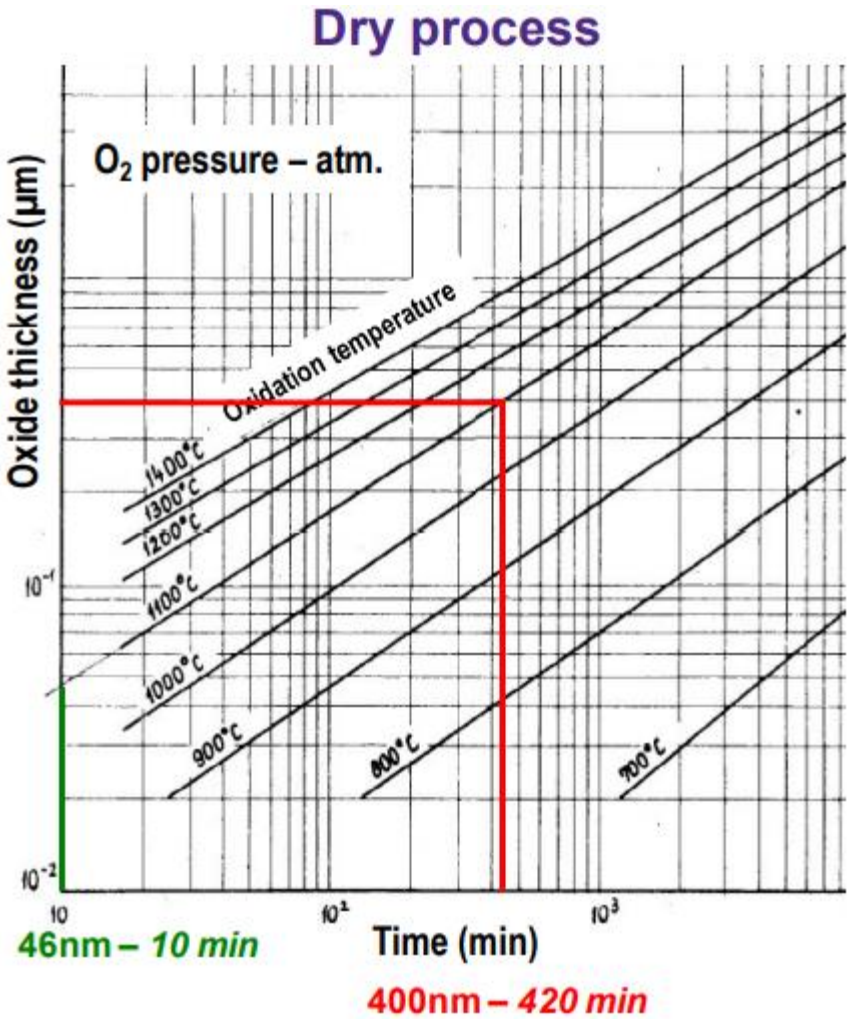
- Oxide is frequently employed as an insulator between two layers of metallization. Oxidation occurs when pure silicon (Si) is exposed to oxygen forming silicon dioxide (SiO_2).

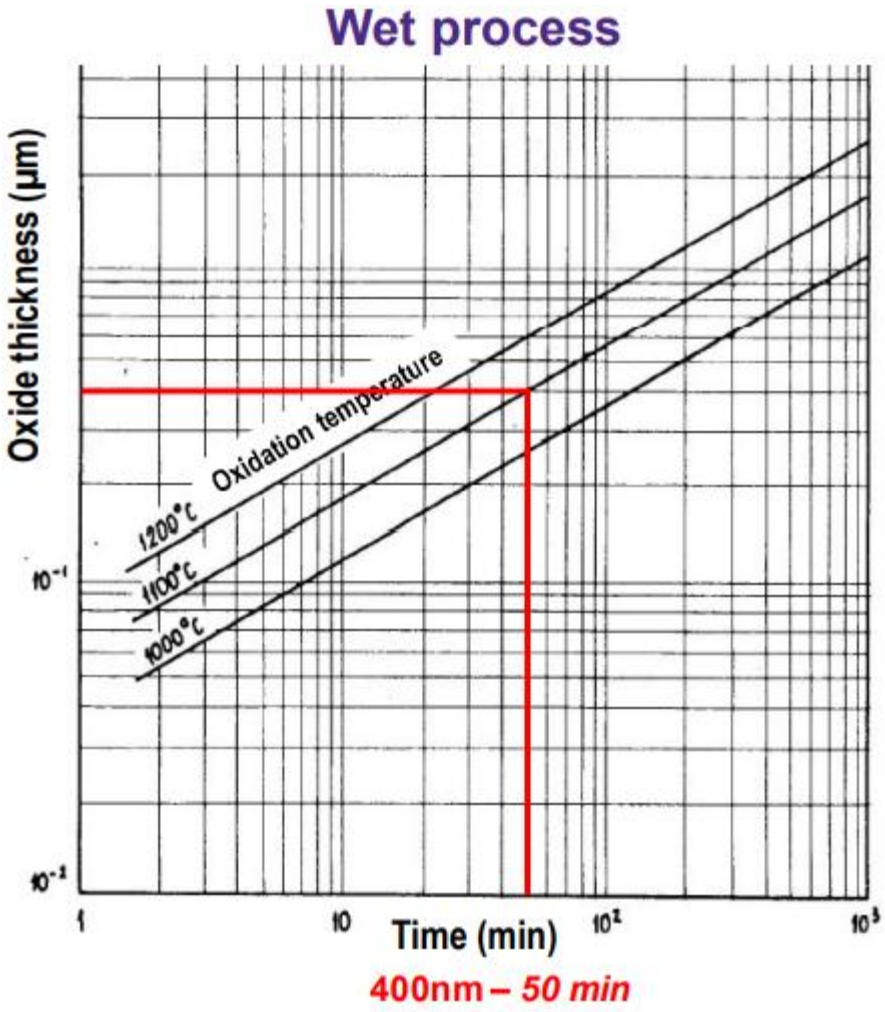
- SiO_2 growth is a key process step in manufacturing all Si devices as it creates extremely high electronic quality gate oxides.



- Characteristics of SIO_2
  - SiO_2 is stable down to 10^{-9} Torr , T > 900°C.
  - SiO_2 can be etched with HF which leaves Si unaffected.
  - SiO_2 is a diffusion barrier for B, P, As.
  - SiO_2 is good insulator, r > 10^{16} ohm-cm.




Dry process
O_2 pressure – atm.
Oxide thickness (μm)
Oxidation temperature
1400°C
1300°C
1200°C
1100°C
1000°C
900°C
800°C
700°C
10^{-1}
10^{-2}
10
10^2
10^3
Time (min)
46nm – 10 min
400nm – 420 min


Wet process
Oxide thickness (μm)
Oxidation temperature
1200°C
1100°C
1000°C
10^{-1}
10^{-2}
1
10
10^2
10^3
Time (min)
400nm – 50 min

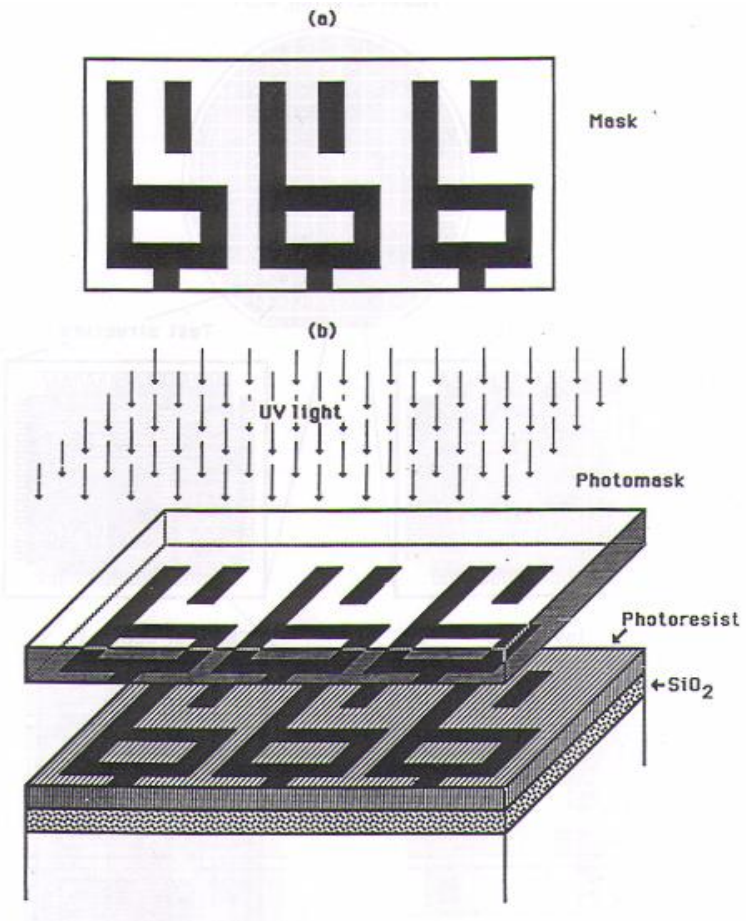
Lithography

- Lithography is the most complicated, expensive, and critical process of modern IC manufacturing. .

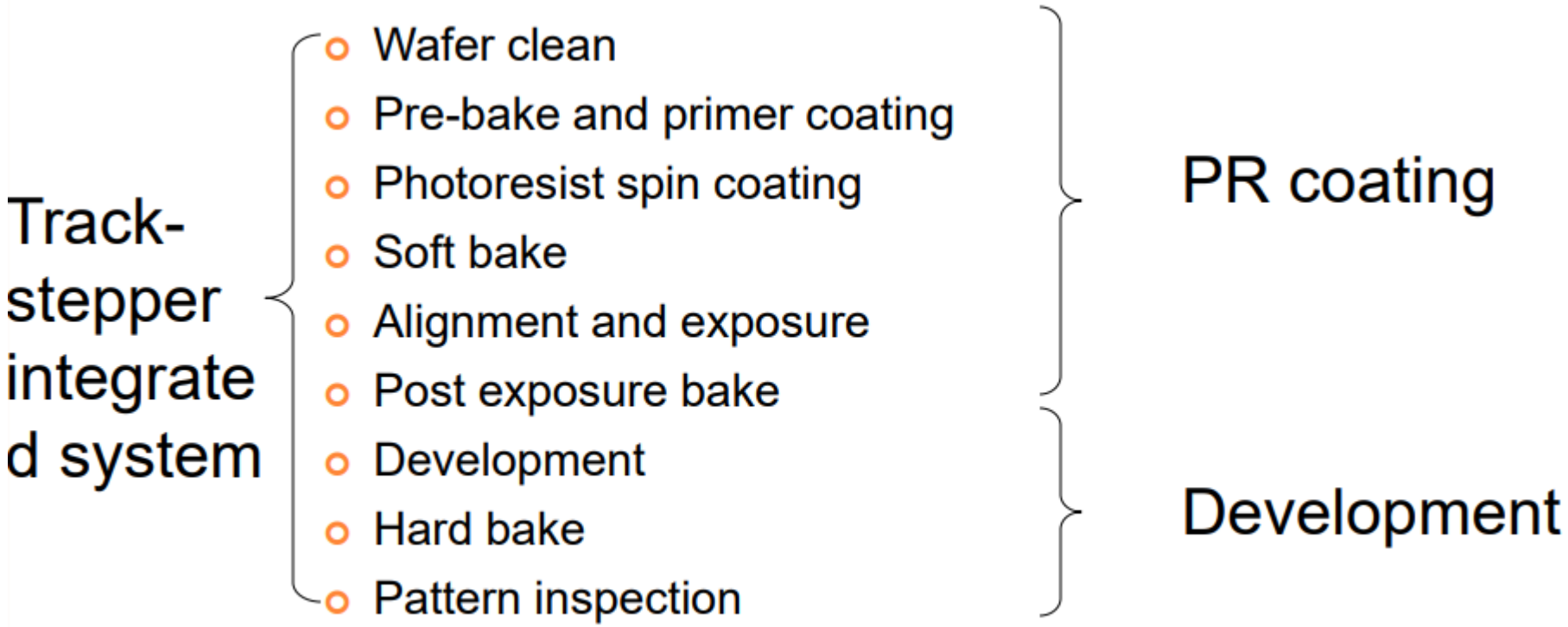
- Lithography transforms complex circuit diagrams into pattern which are define on the wafer to form a number of superimposed layers of insulator, conductor and semiconductors materials.

- The minimum feature size i.e., the minimum line width or line to line separation that can be printed on the surface, control the number of circuits that can be placed on the chip and has a direct impact on circuit speed. The evolution of IC is therefore closely linked to the evolution of lithographic tools.

- A special agent called a photoresist is deposited on the surface. The photoresist is exposed to light through a mask, it changes its properties in a pattern.



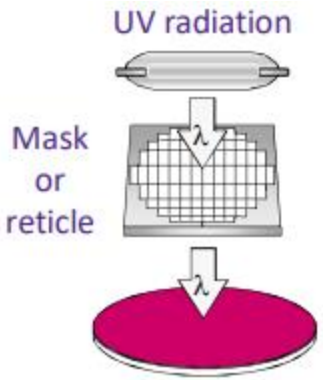
Basic Steps of the Advanced Technology



1) Dehydration

2) Resist spin-on

3) Softbake



4) Alignment and exposure

5) Post-Exposure Bake
(depending on resist)

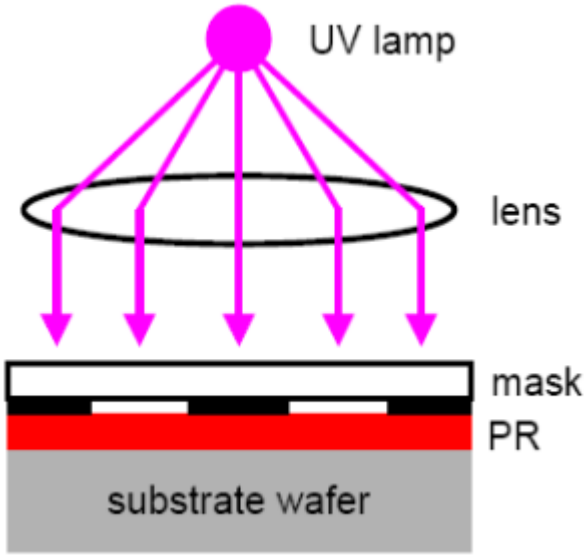
6) Development

7) Hardbake
(depending on resist
and application)

8) Verification of the developed
structure

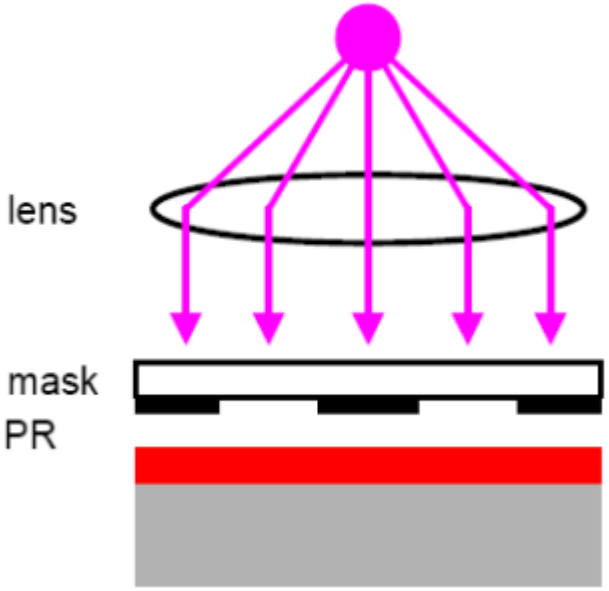
Mask Alignment & Exposure

- Contact Alignment: Resist is in contact with the mask, 1:1 magnification
  - Advantages: Inexpensive equipment and moderately high resolution.
  - Disadvantages: Contact with the mask degrades the mask (pinholes and scratches are created on the metal-oxide layers of the mask and particles or dirt are directly imaged in the wafer).

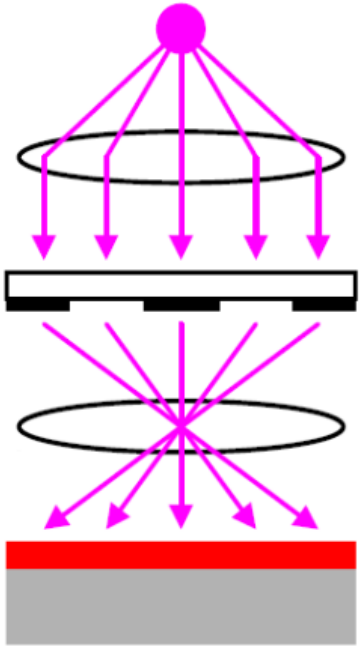


- Proximity Alignment: : Resist is almost, but not in contact with the mask, 1:1 magnification

  - Advantages: Inexpensive equipment, low resolution (~1-2 um or slightly better) and Longer mask lifetime.
  - Disadvantages: Diffraction effects limit accuracy of pattern transfer. Less repeatable than contact methods.

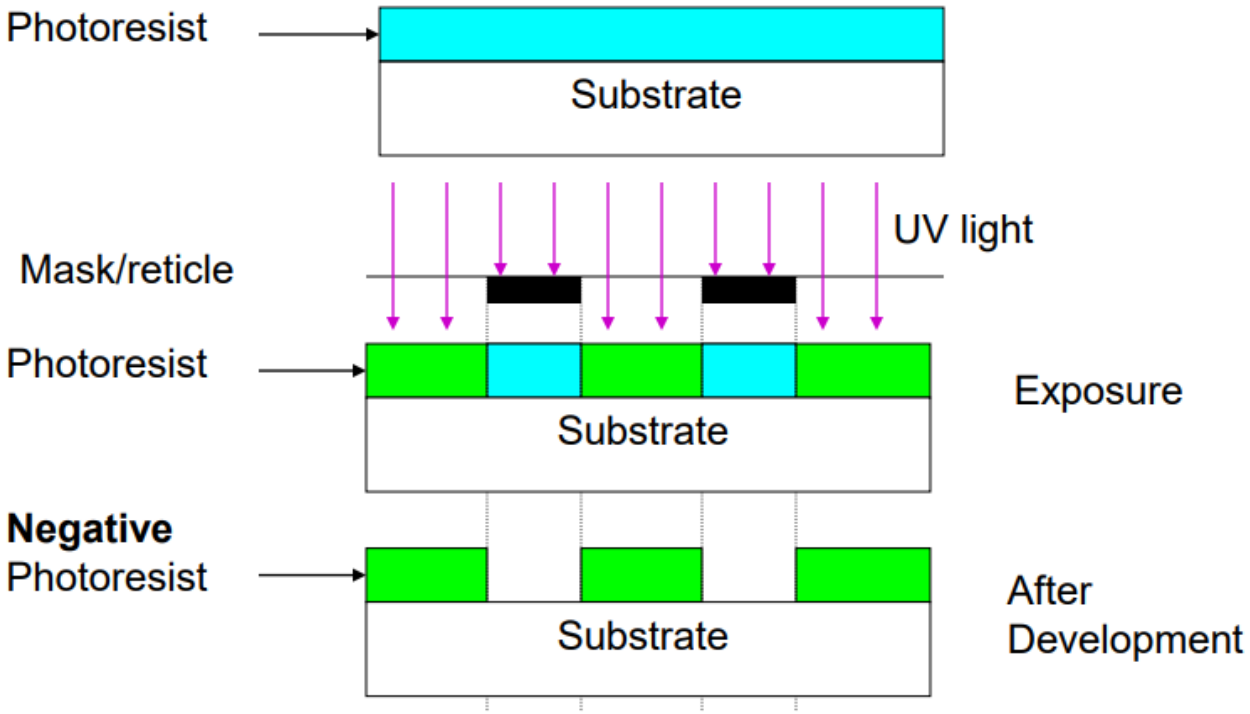


- Projection Alignment : Mask image is projected a distance from the mask and de-magnified to a smaller image, 1:4 -1:10 magnification
  - Advantages: Can be very high resolution (~0.007 um or slightly better), No mask contact results in almost no mask wear (high production compatible), mask defects or particles on mask are reduced in size on the wafer.
  - Disadvantages: Extremely expensive and complicated equipment, diffraction effects limit accuracy of pattern transfer.

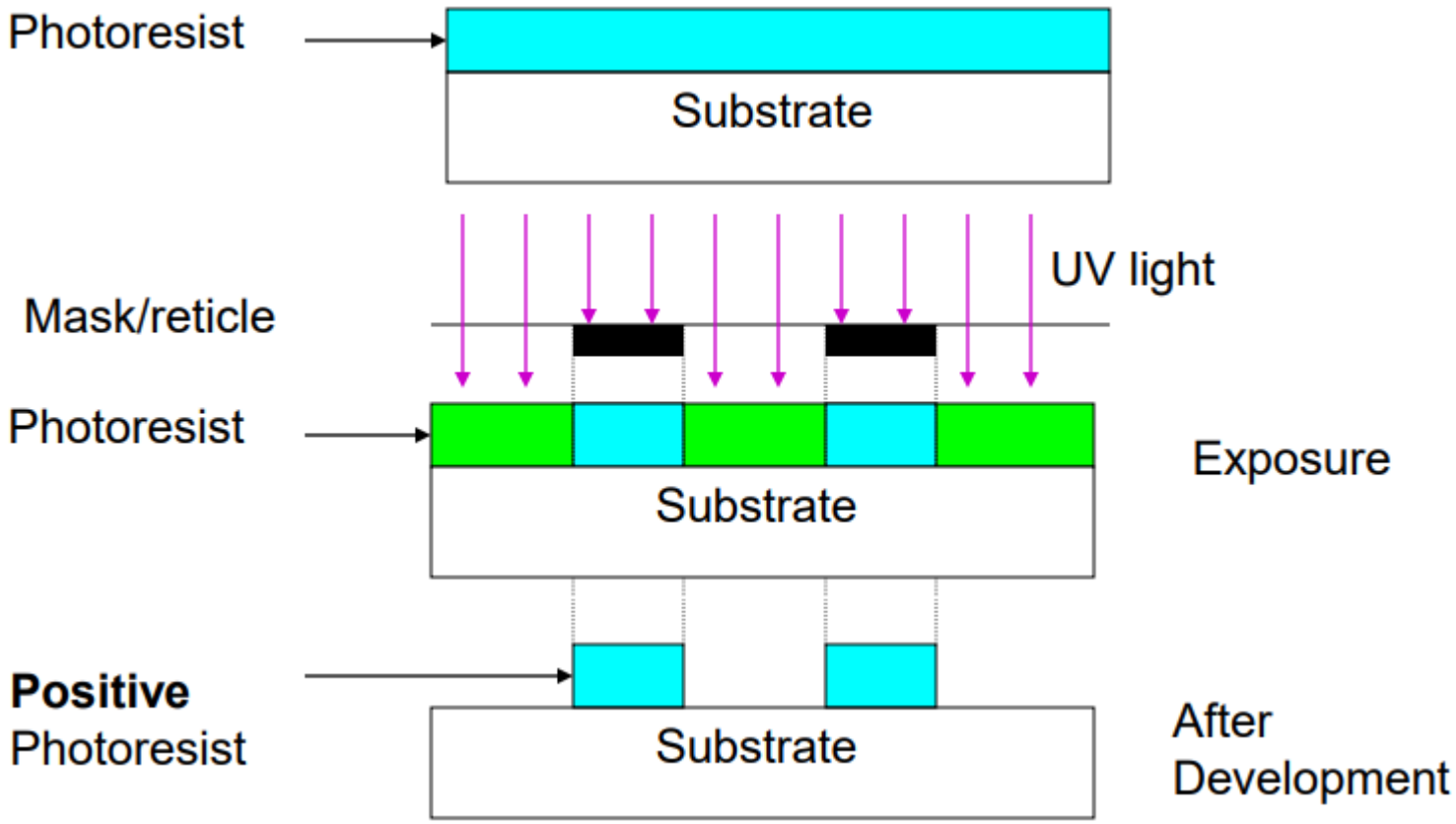


Types of Photoresist

- Negative Photoresist
  - Becomes insoluble after exposure
  - When developed, the unexposed parts dissolved.
  - Cheaper



- Positive Photoresist
  - Becomes soluble after exposure
  - When developed, the exposed parts dissolved
  - Better resolution



Etching

- After a thin film is deposited, it is usually etched to remove unwanted materials and leave only the desired pattern on the wafer. The process is done many times.

- In addition to deposited films, sometimes we also need to etch the Si wafer to create trenches (especially in MEMS).

- The masking layer may be photoresist, SiO_2 or Si_3N_4. The etch is usually done until another layer of a different material is reached

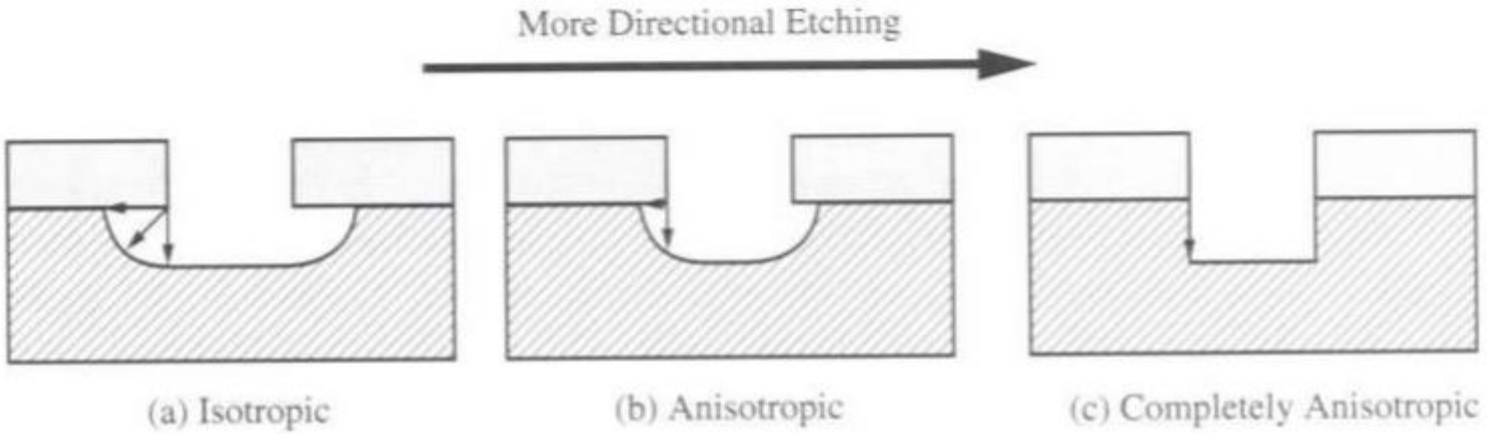
Etching Types

- Etching can be done “wet” or “dry”

  - Wet etching
    - Uses liquid etchants
    - Wafer is immersed in the liquid
    - Process is mostly chemical
    - Wet etching is not used much in VLSI wafer fabrication.

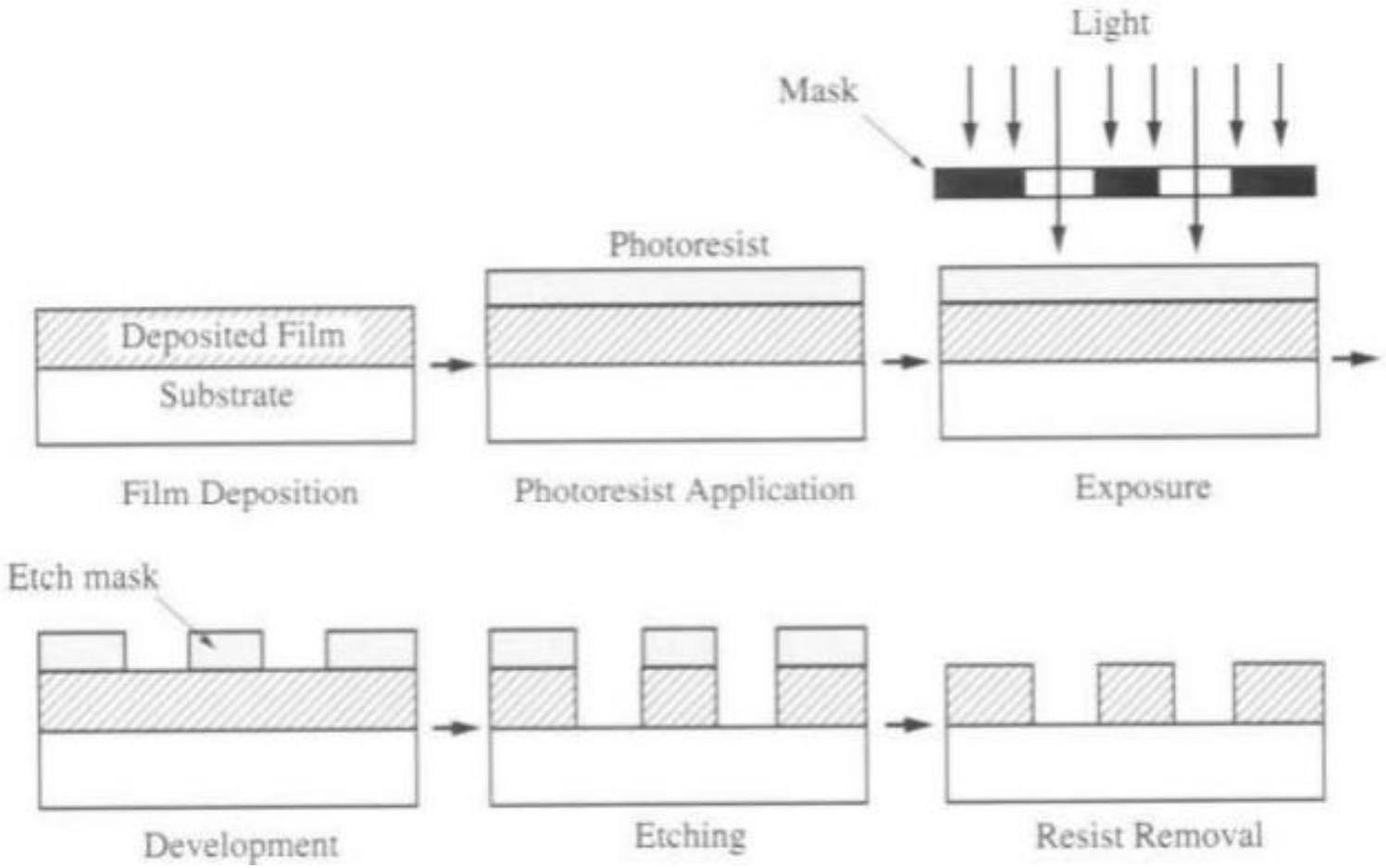
  - Dry etching
    - Uses gas phase etchants in a plasma
    - The process is a combination of chemical and physical action.
    - Process is often called “plasma etching”.
    - This is the normal process used in most VLSI fabrication.

- Etch directionality is a measure of the etch rate in different directions (usually vertical versus lateral)



- Uniform etching speed in all directions
- Under etching

- Different etching speed in different directions.
- Etching profile depends on the wafer orientation


Light
Mask
Photoresist
Deposited Film
Substrate
Film Deposition
Photoresist Application
Exposure
Etch mask
Development
Etching
Resist Removal

Budapest University of Technology and Economic
Department of Electron Devices

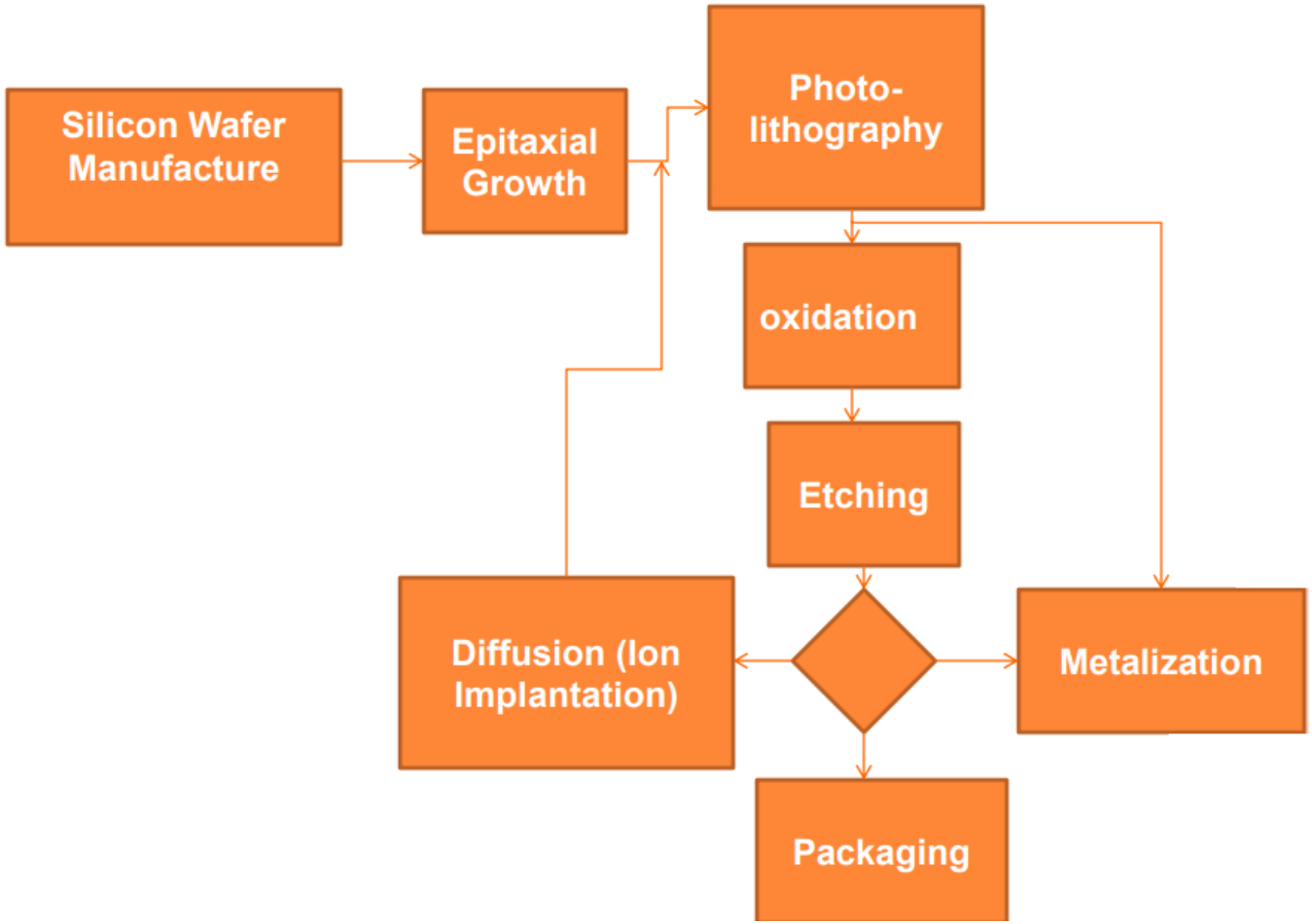
Circuit Environment

Lecture 3

- **Fabrication Processes**
- **Fabrication of MOSFET Transistor**
- **Fabrication of CMOS Transistor**

Ahmed I Alnahhal

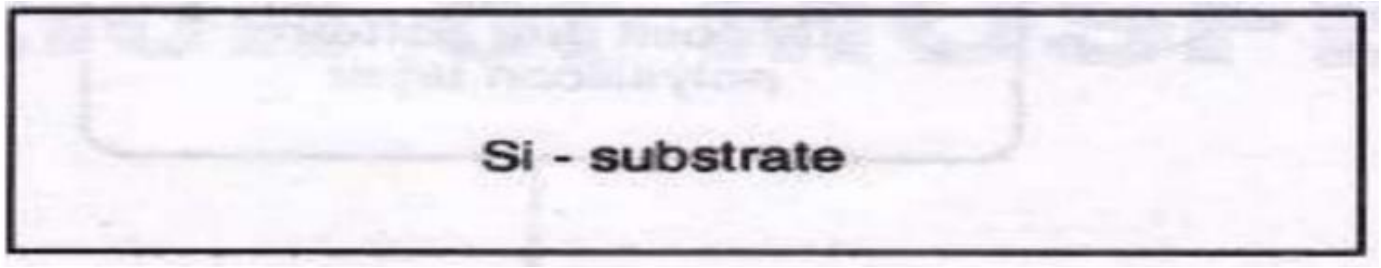
FABRICATION PROCESSES FOR VLSI DEVICES



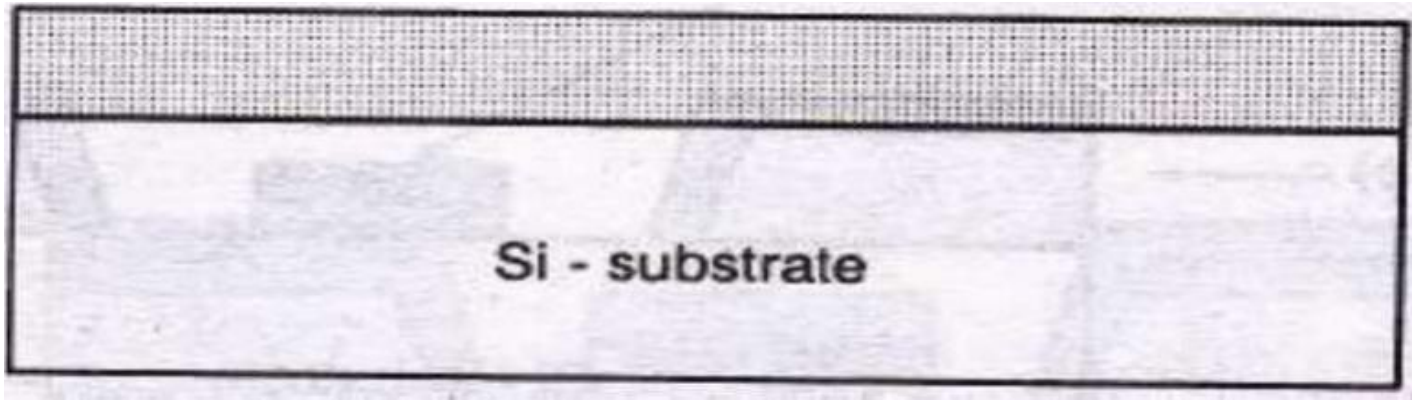
Fabrication of MOSFET Transistor

- Fabrication process sequence for NMOS

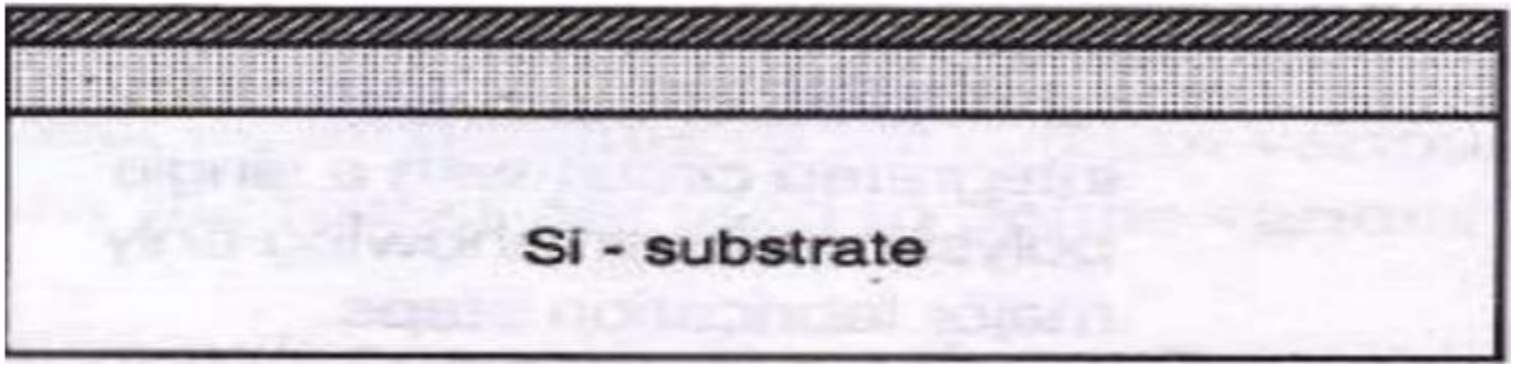
1. The starting Si wafer is a lightly doped p – type substrate.



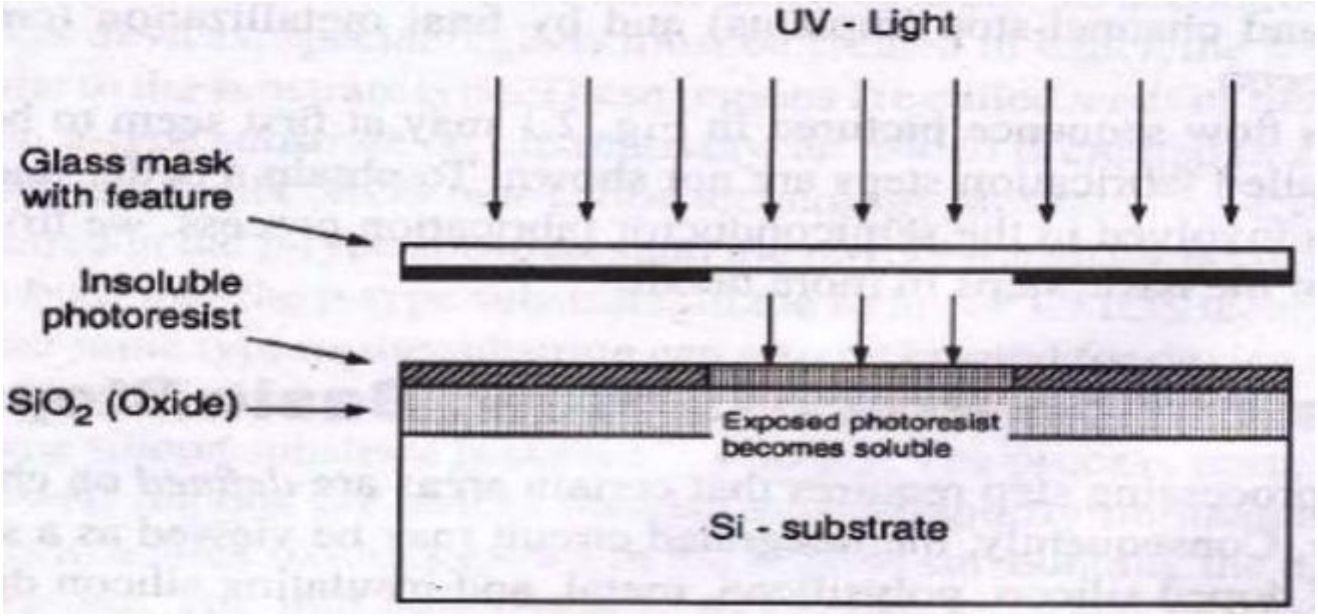
2. First step is to oxidize the Si to form a layer of SiO_2



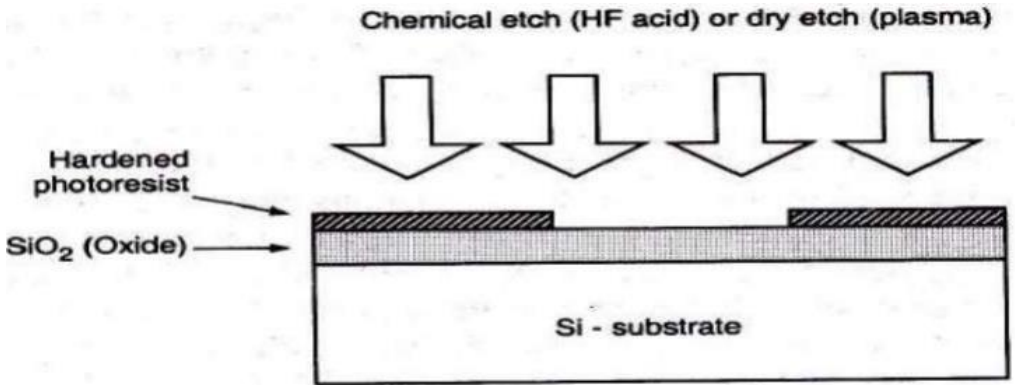
3. Coat the Si with photoresist.



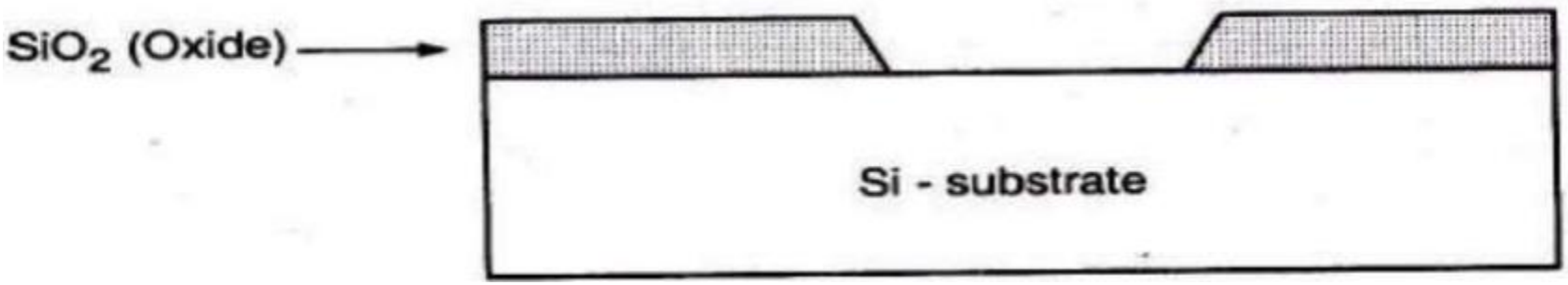
4. The next step is lithography in order to form source and drain regions.



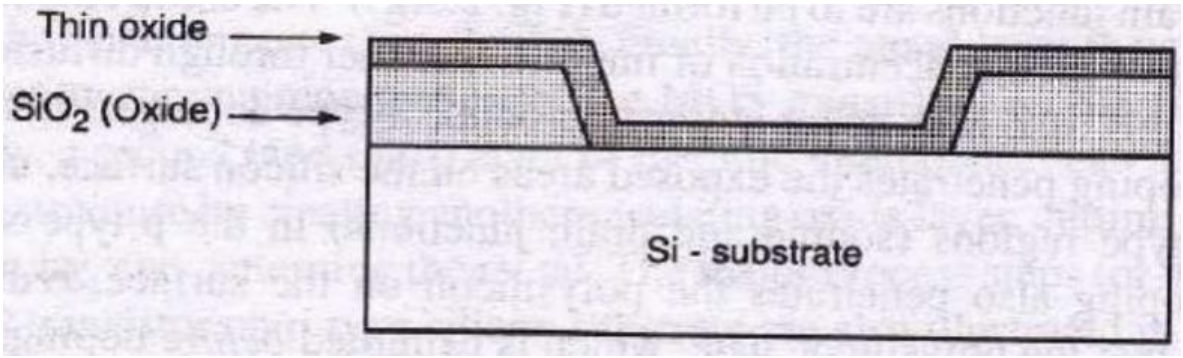
5. The SiO_2 regions which are not covered by hardened photoresist can be etched away either by chemical etching or dry etching.



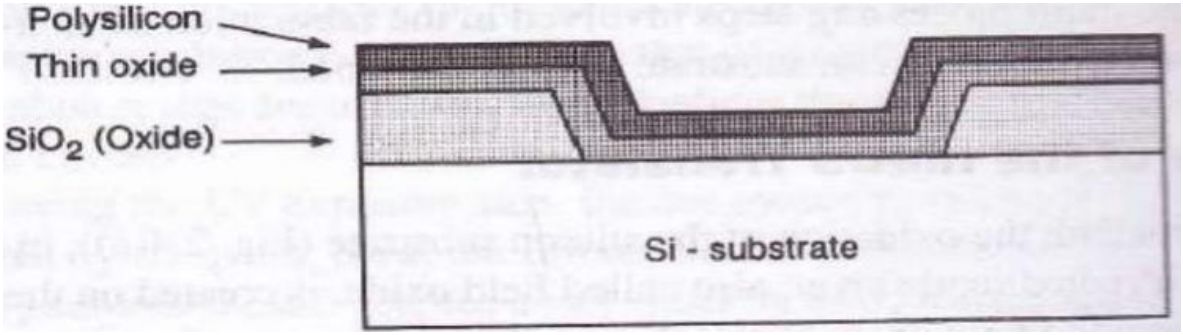
6. The remaining photoresist can be removed by using another solvent.



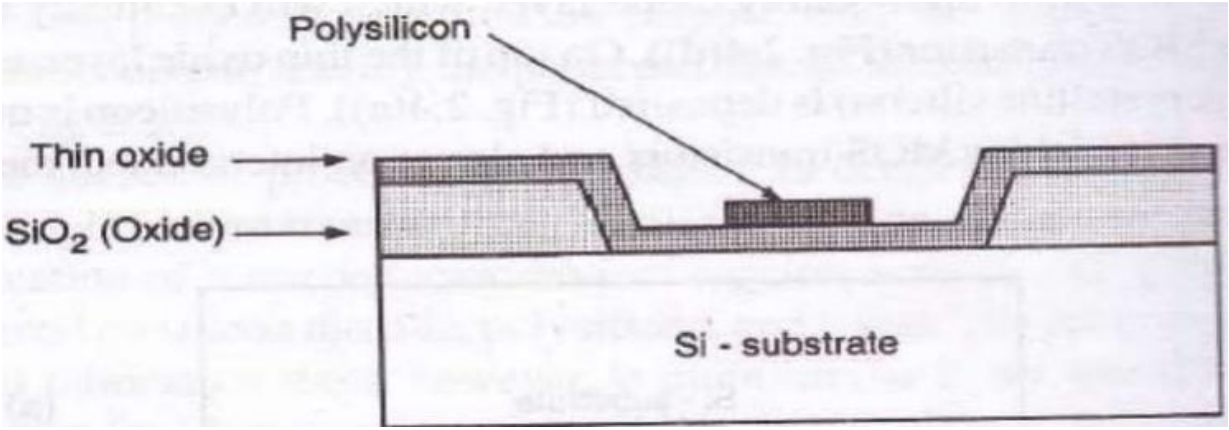
7. Deposit a layer of thin oxide in order to form gate oxide of the NMOS transistor



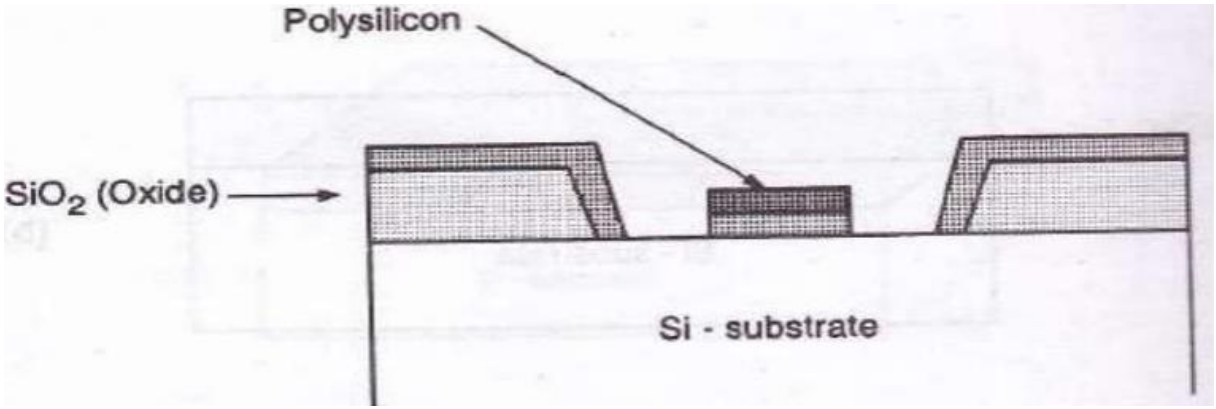
8. A layer of polysilicon is deposited. It is used as gate electrode material for MOS to interconnect it.



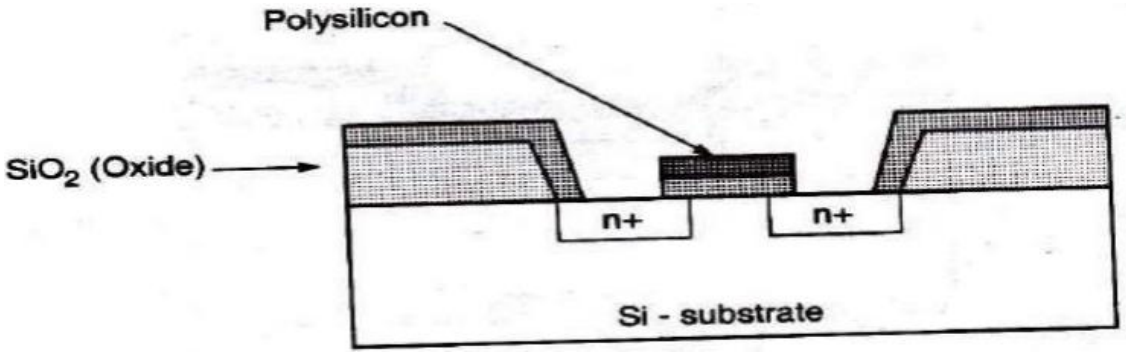
9. The polysilicon layer is patterned and etched to form the interconnects and the MOS transistor gate.



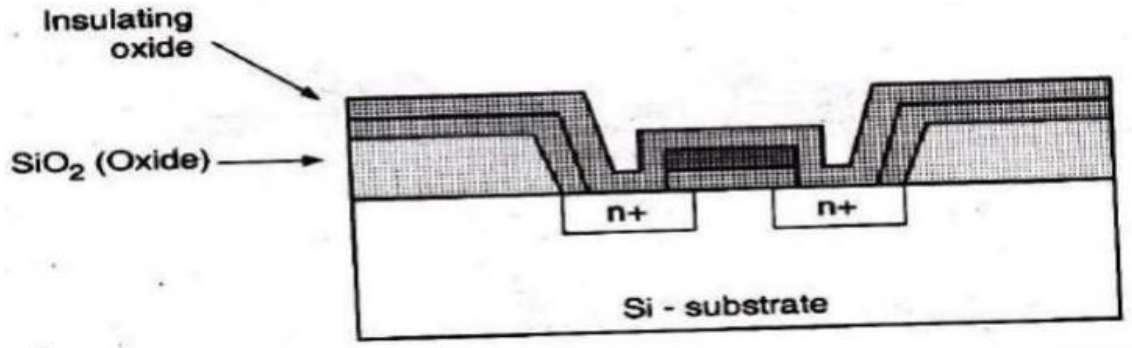
10. The thin oxide not covered by polysilicon is also etched away so that source and drain junctions may be formed.



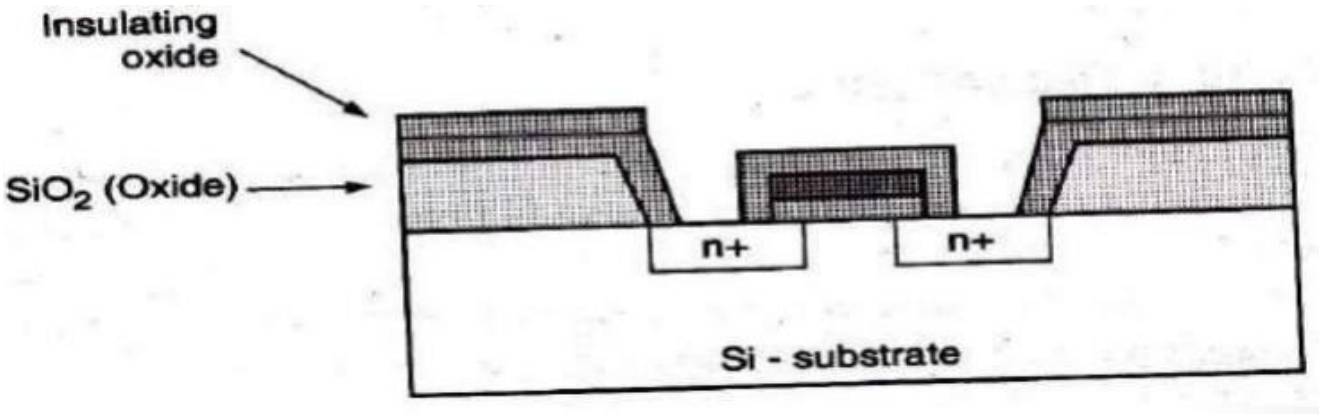
11. The entire silicon surface is then doped with a high concentration of impurities either by diffusion or ion implantation.



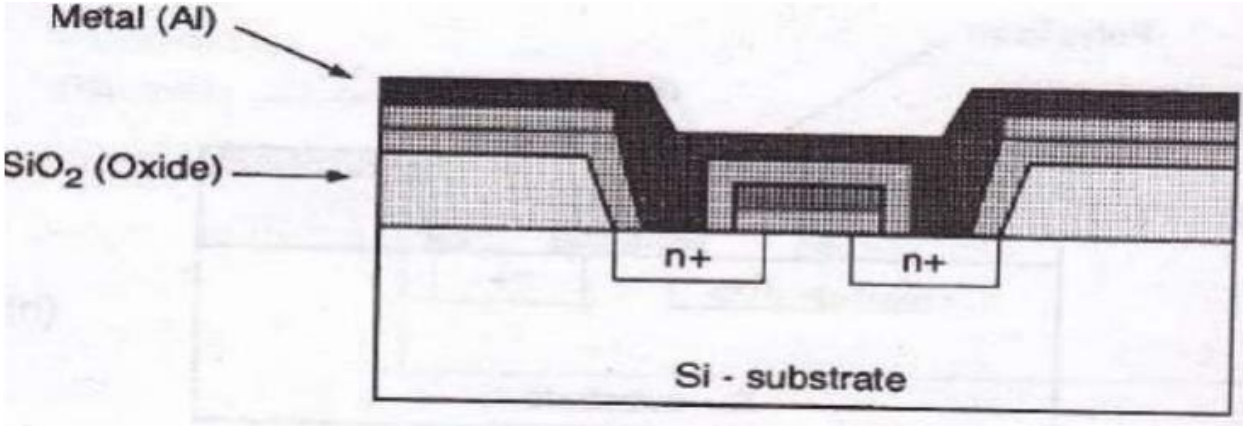
12. Once the source and drain regions are completed, the entire surface is again covered with and insulating layer of SiO_2 .



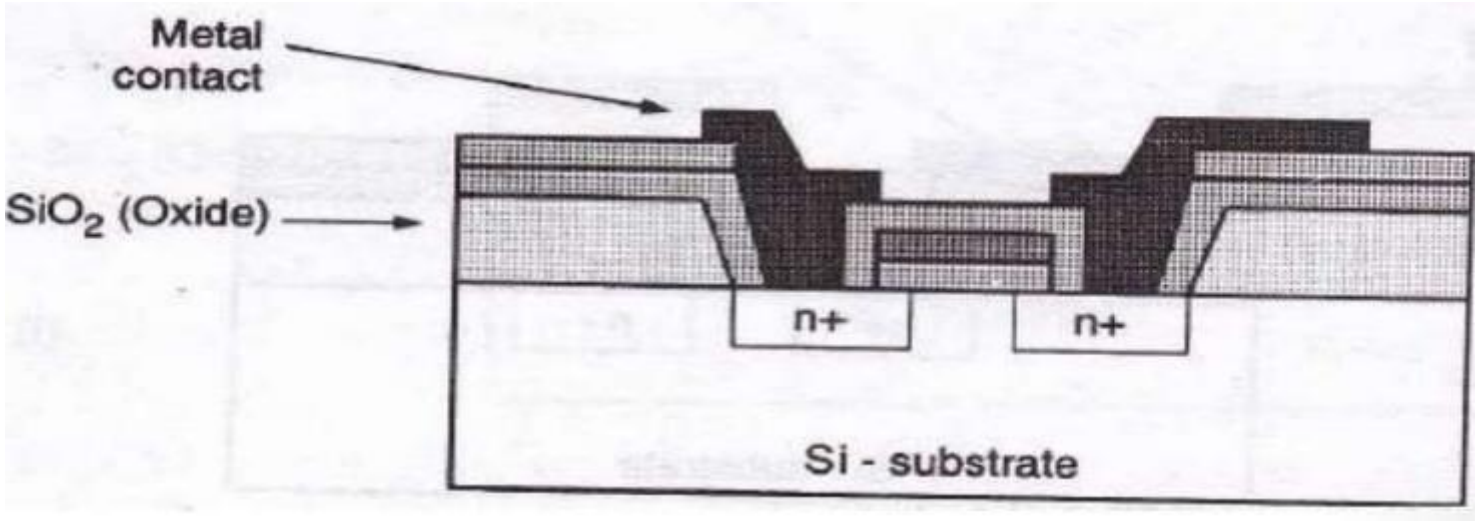
13. The insulating oxide is then patterned in order to provide contact window for drain and source junctions.



14. The surface is now covered with evaporated aluminium which will form the interconnections.

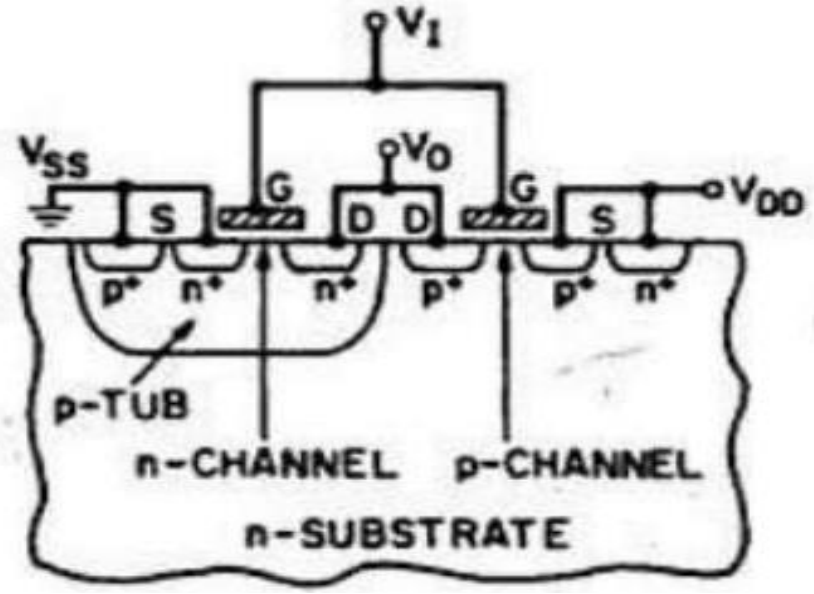


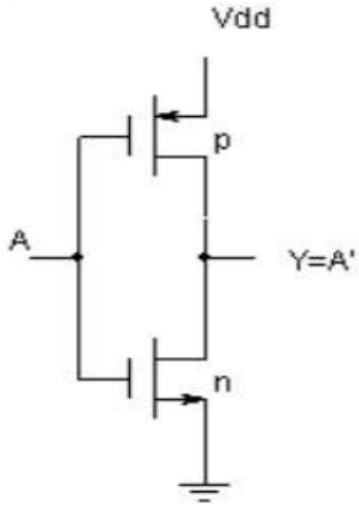
15. Finally the metal layer is patterned and etched, completing the interconnections of the MOS transistor on the surface.



CMOS Transistor Technology

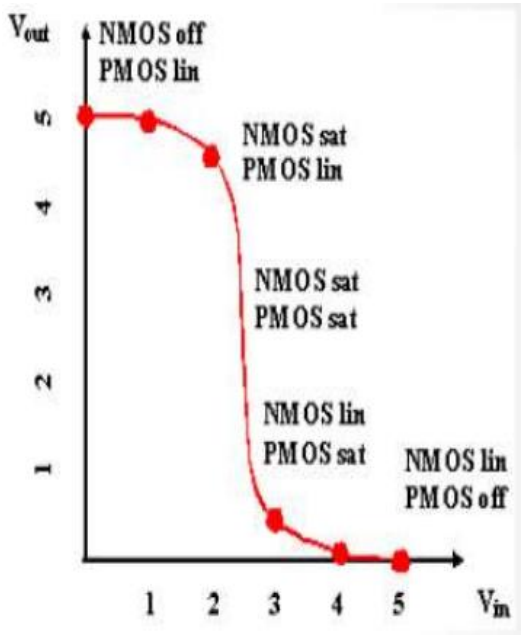
- A CMOS inverter is realized by the series combination of a PMOS and NMOS transistors.
- The cross section of the inverter structure shows the n-channel transistor formed in a p-region called tub or well. The gates of the transistors are connected to from the input.





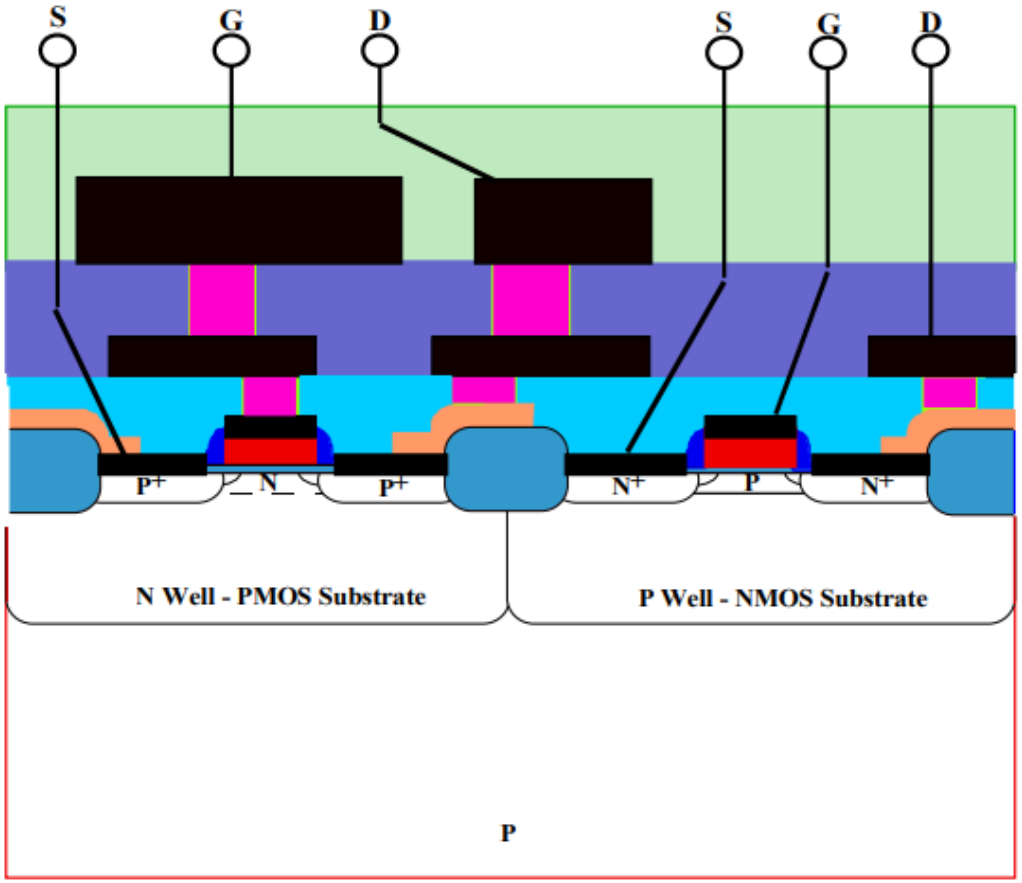
- Transfer characteristic of the CMOS inverter is output voltage as a function of input voltage.

- In order to understand the operation of the CMOS inverter, define the threshold voltages of NMOS and PMOS transistors. Let V_{Tn} = 1 V & V_{Tp} = -1 V and V_{DD} = 5V.

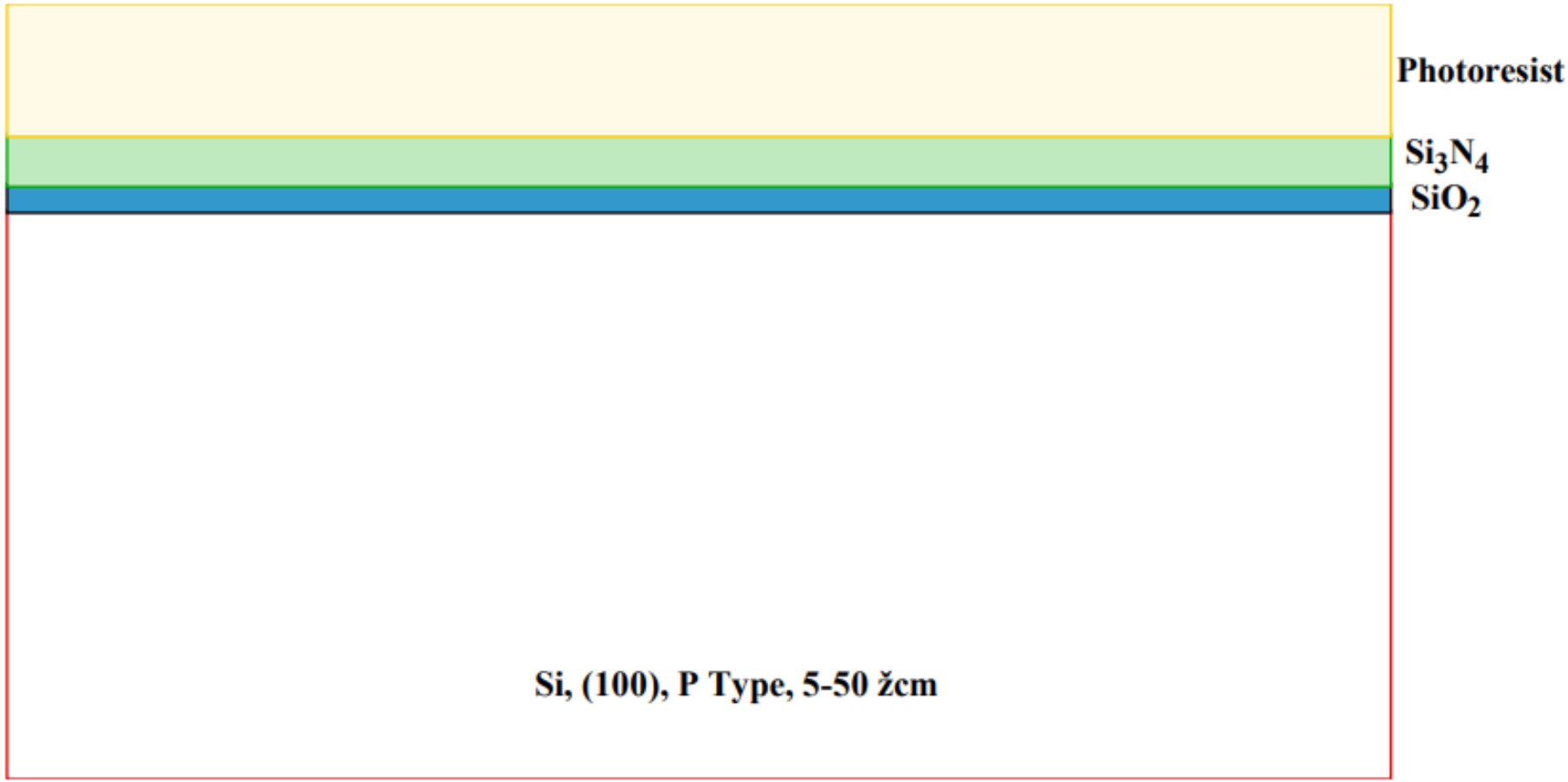


Fabrication of CMOS transistor

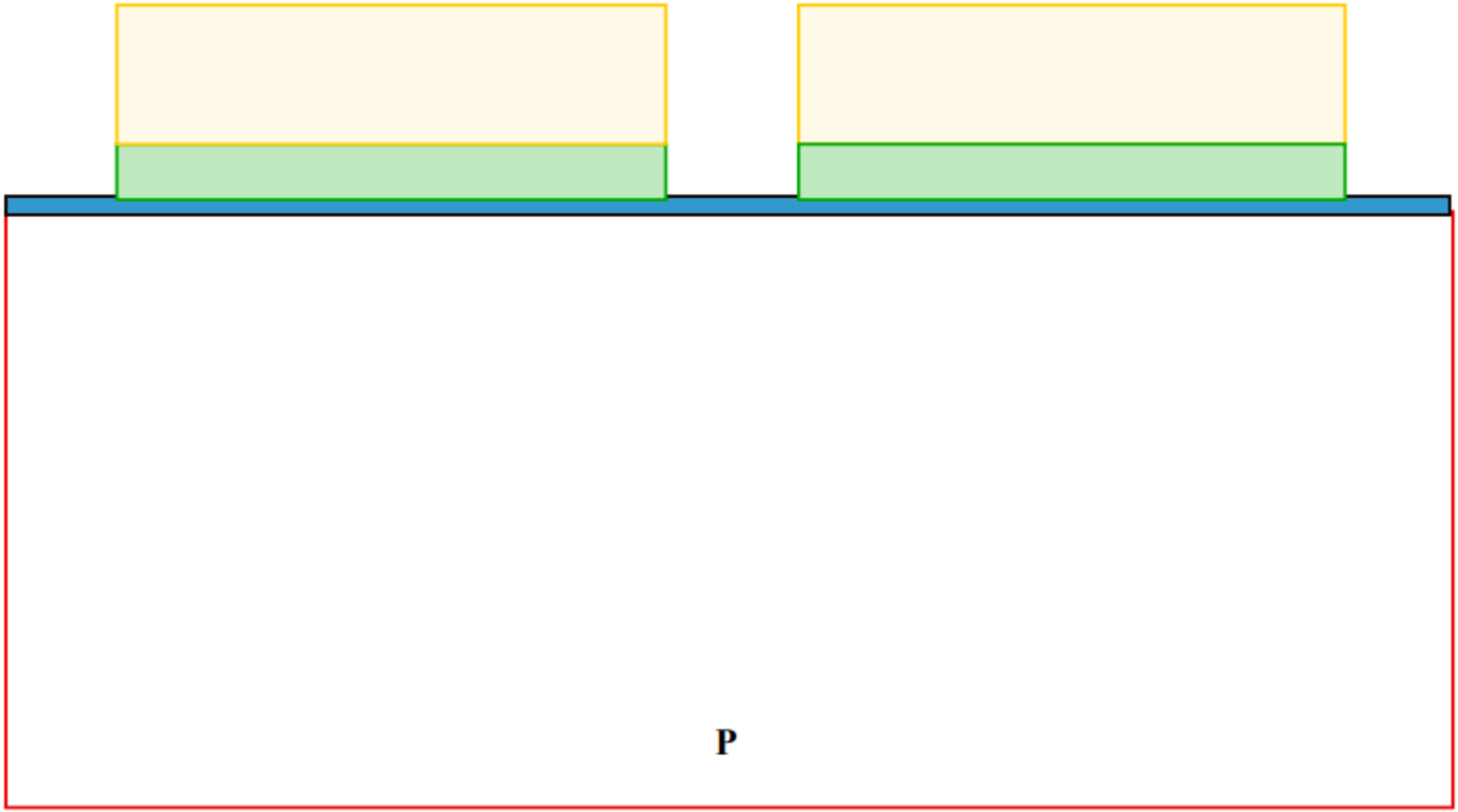
Cross sectional view of final CMOS circuits



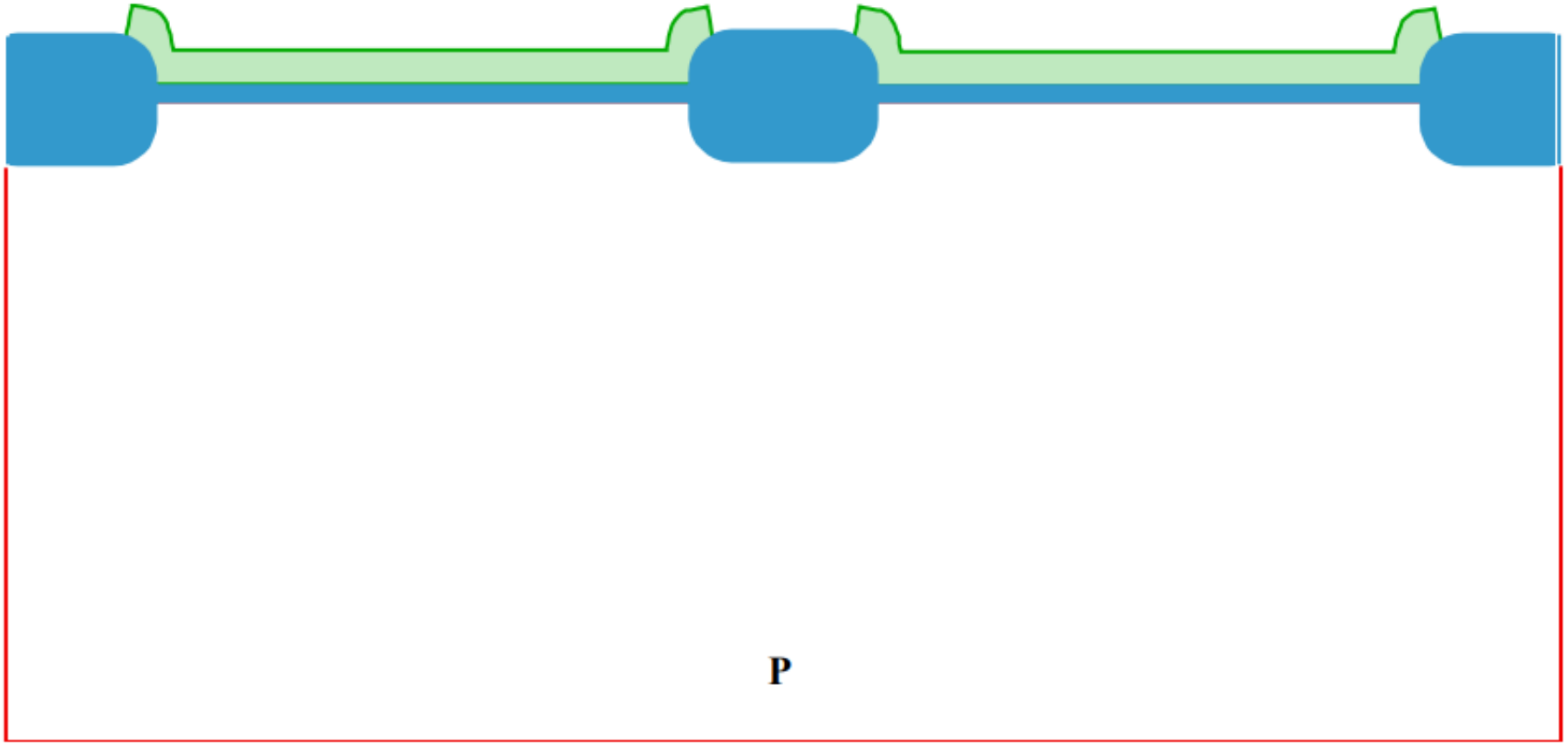
CMOS Process Flow



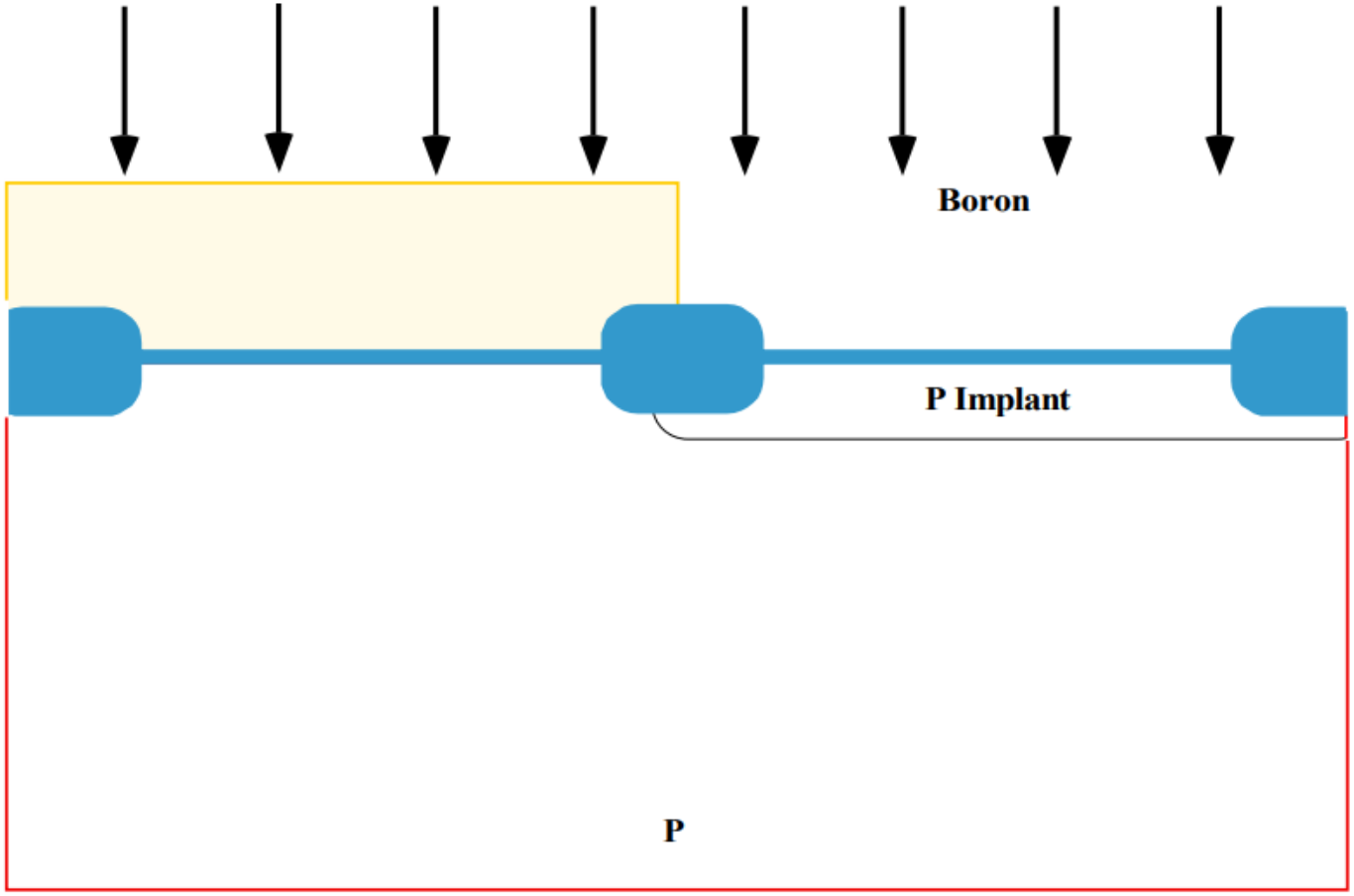
Mask #1 patterns the active areas. The nitride is dry etched.



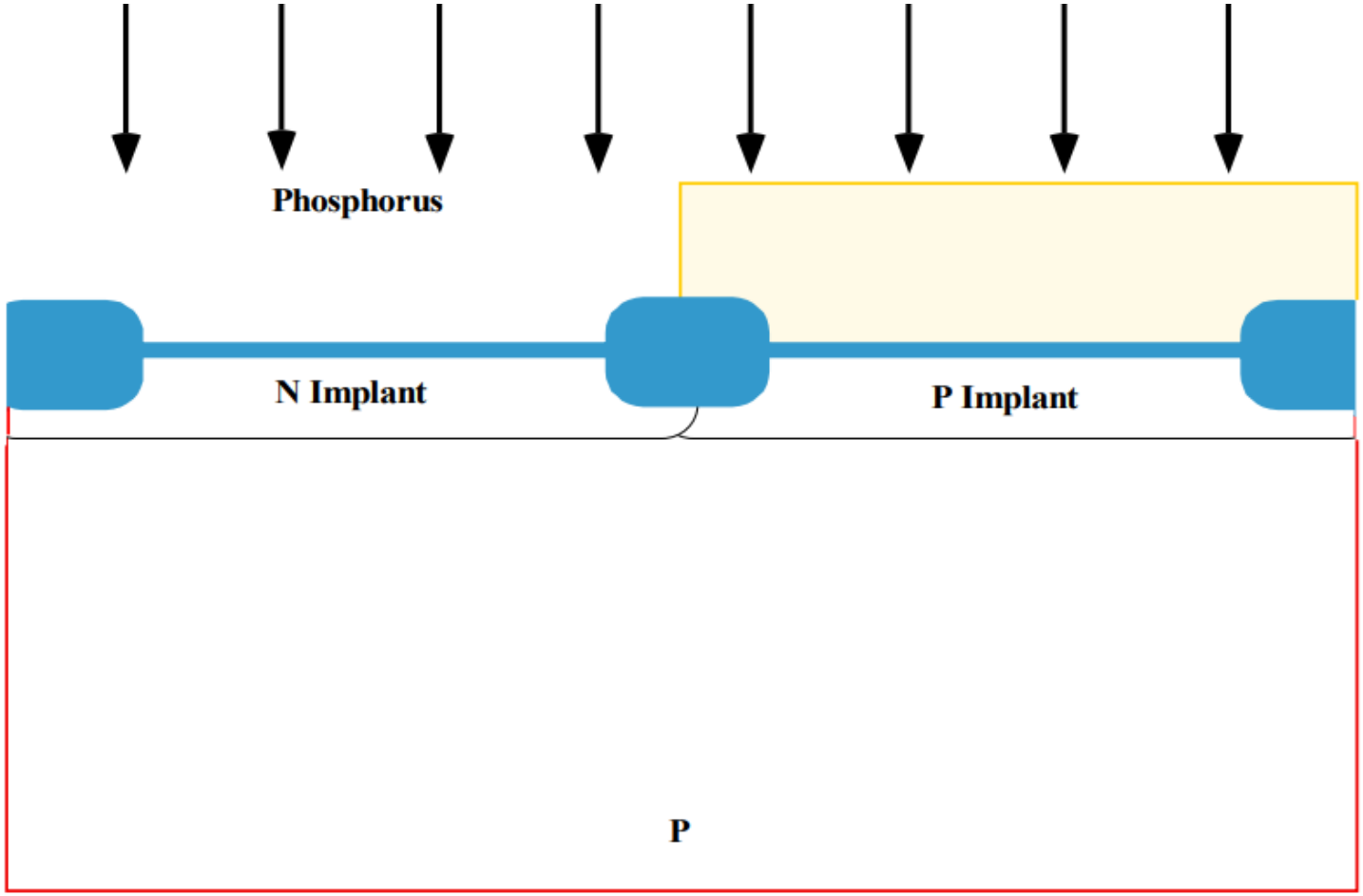
Field oxide is grown using a LOCOS process. Typically 90 min @ 1000 ˚C in H_2O grows ≈ 0.5 µm.



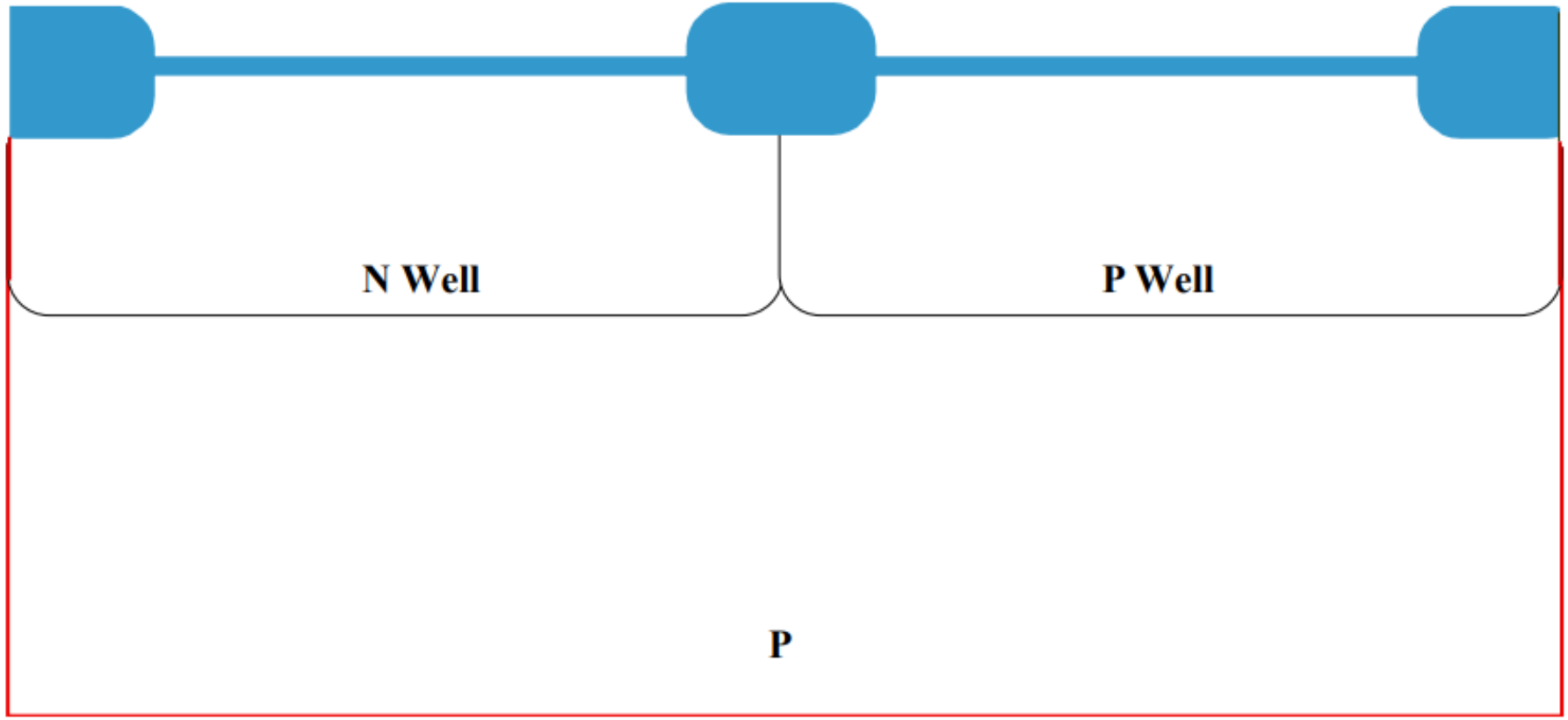
Mask #2 blocks a B^+ implant through the PMOS and just to form the wells for the NMOS devices. Typically, 10^{13} cm^{-2} @ 150-200 KeV.



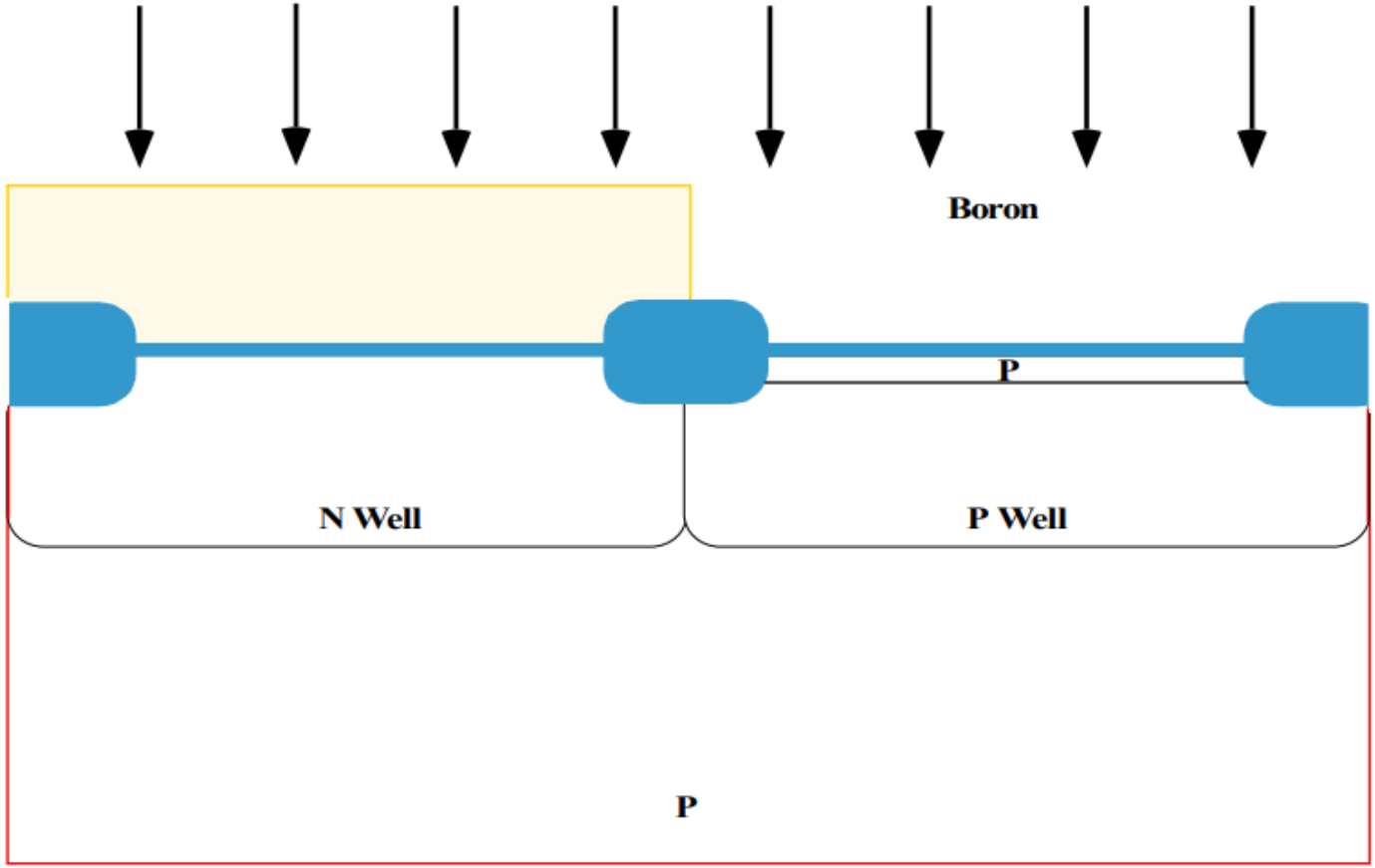
Mask #3 blocks a P^+ implant through the NMOS and just to form the wells for the PMOS devices. Typically, 10^{13} cm^{-2} @ 300 KeV.



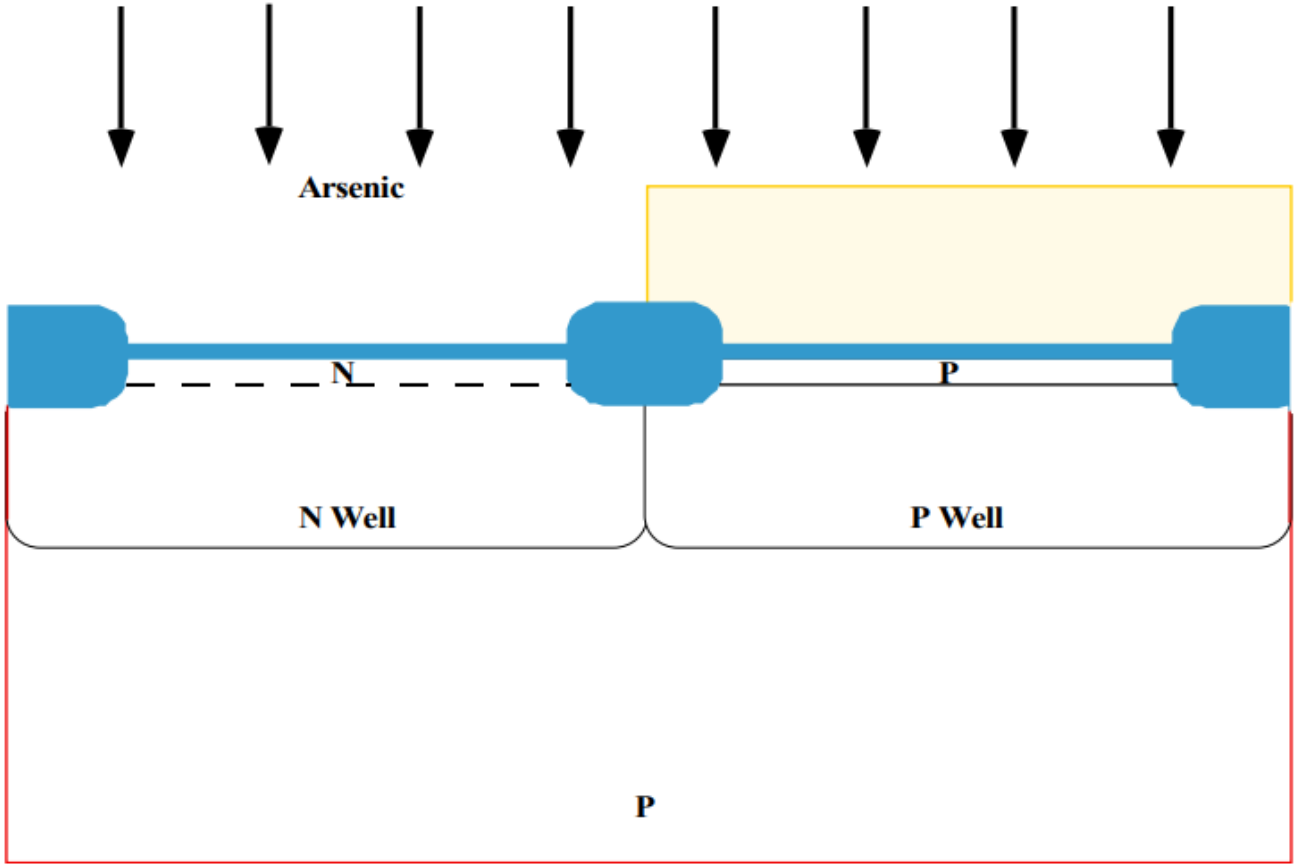
A high temperature drive-in produces the “final” well depths and repairs implant damage. Typically, 4-6 hours @ 1000 ˚C - 1100 ˚C.



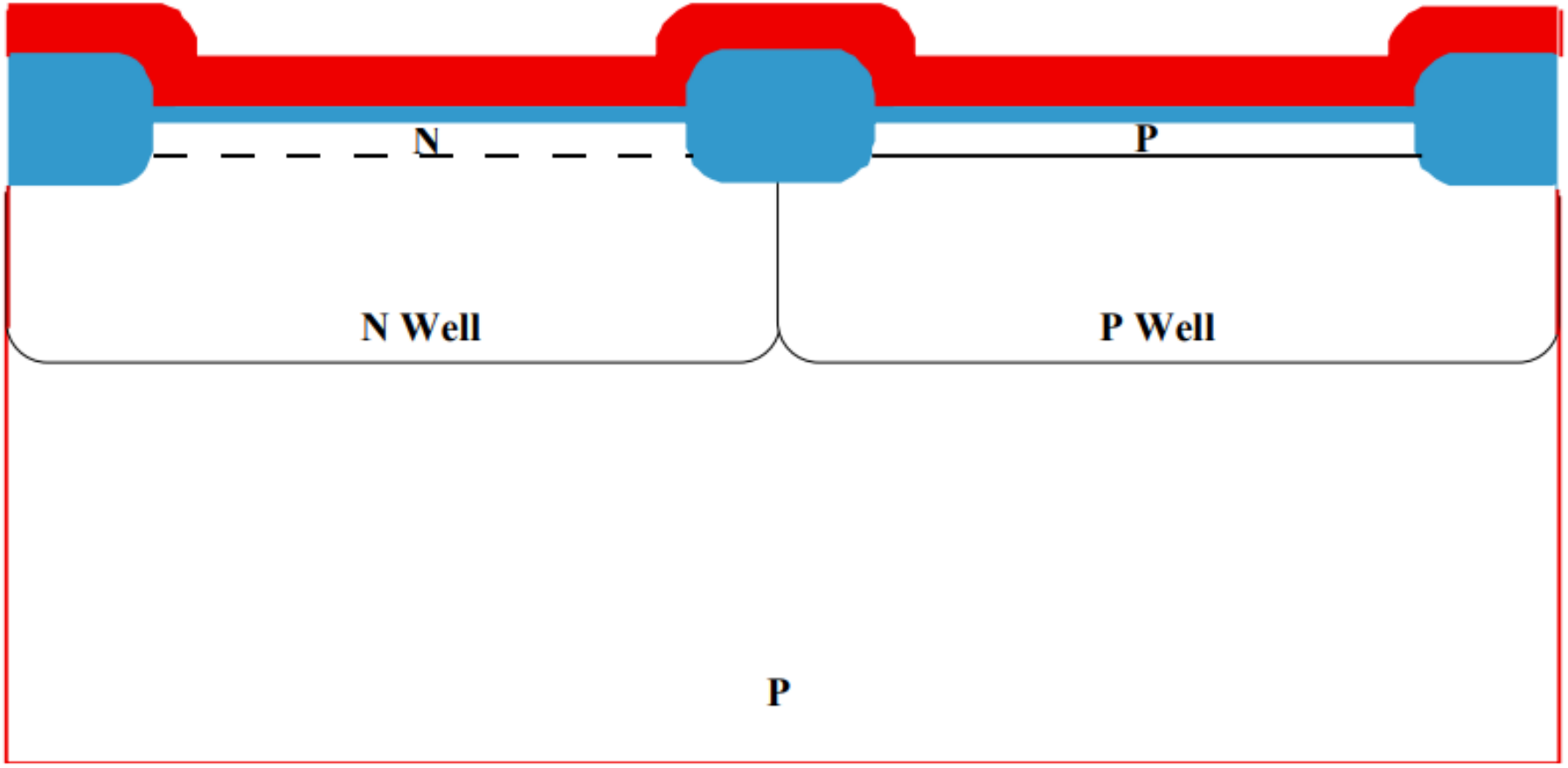
Mask #4 is used to mask the PMOS devices. A V_{TH} adjust implant is done on the NMOS devices, typically a 1-5 x 10^{12} cm^{-2} B+ implant @ 50 - 75 KeV.



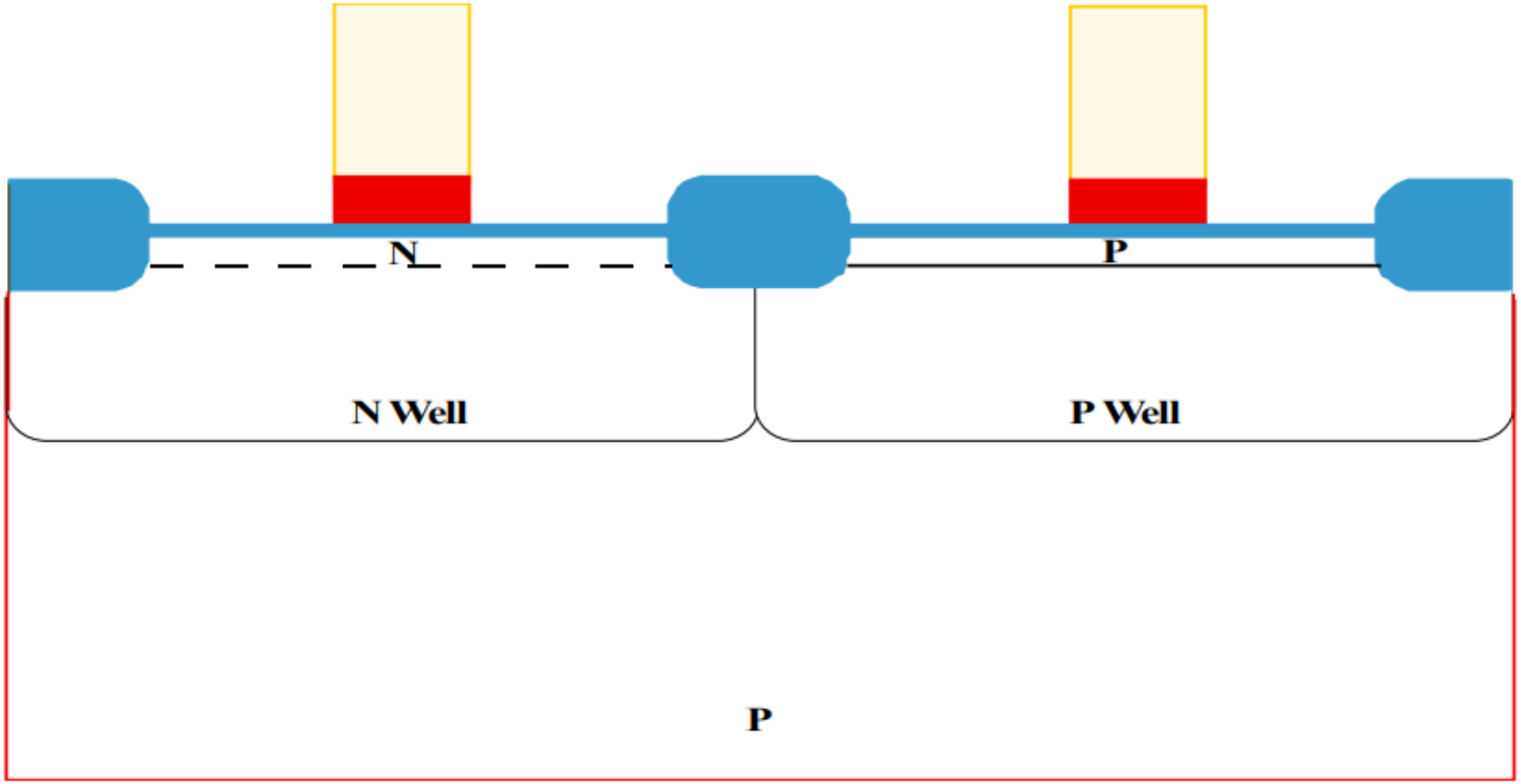
Mask #5 is used to mask the NMOS devices. A V_{TH} adjust implant is done on the PMOS devices, typically 1-5 x 10^{12} cm^{-2} As+ implant @ 75 - 100 KeV.



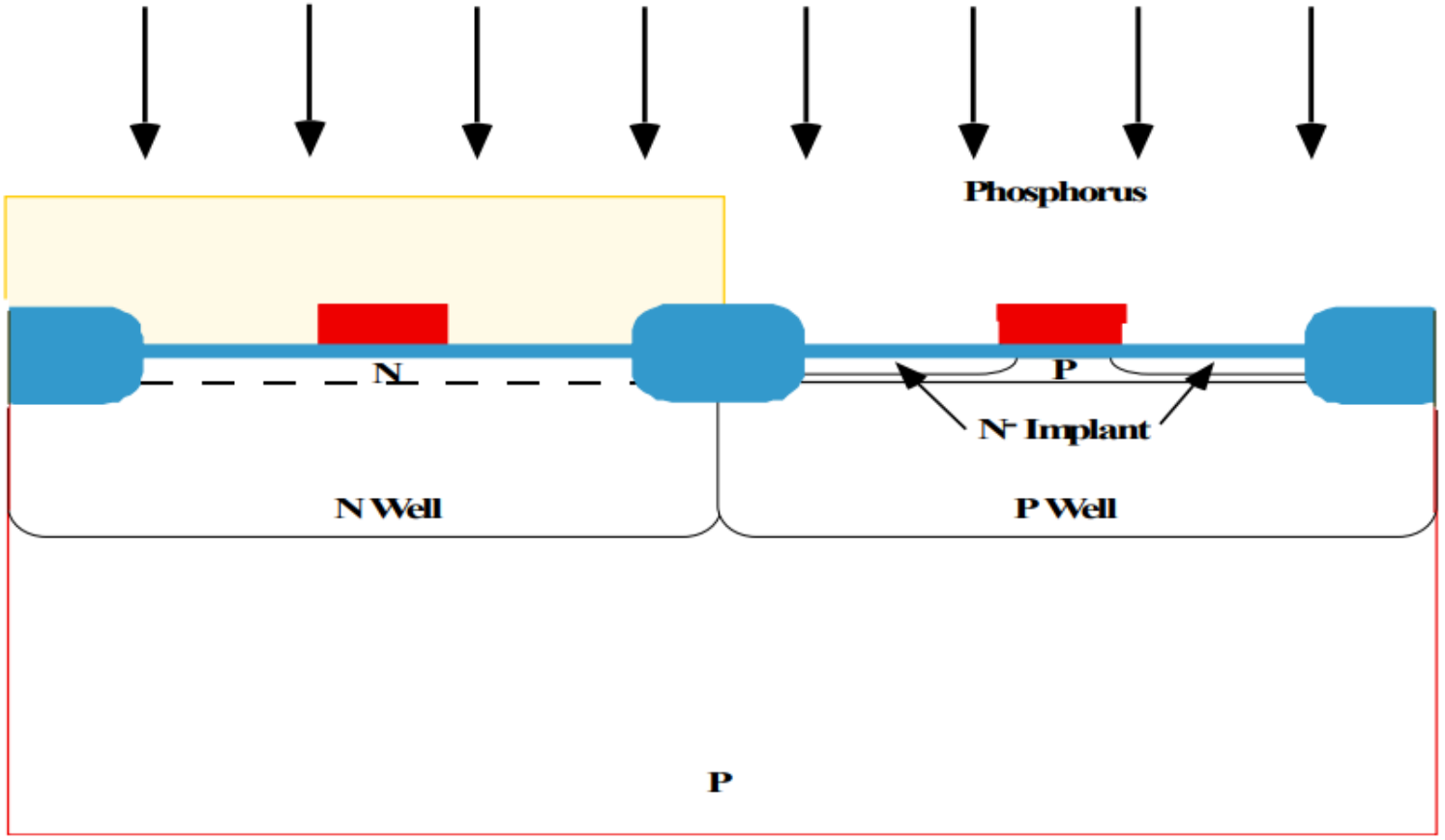
Polysilicon is deposited by LPCVD (≈ 0.5 µm). An unmasked P^+ or As^+ implant dopes the poly (typically 5 x 10^{15} cm^{-2}).



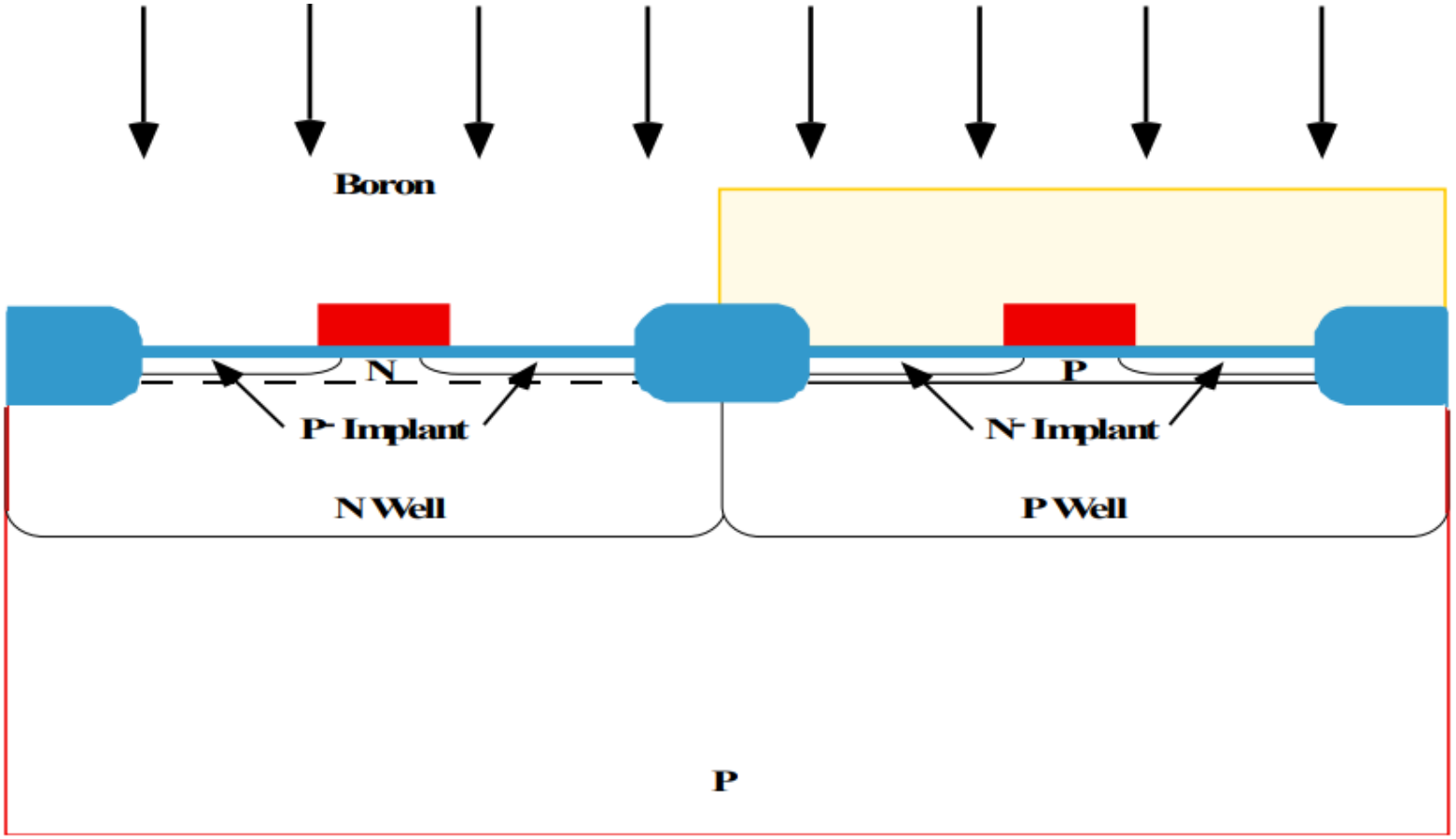
Mask #6 is used to protect the MOS gates. The poly is plasma etched using an anisotropic etch.



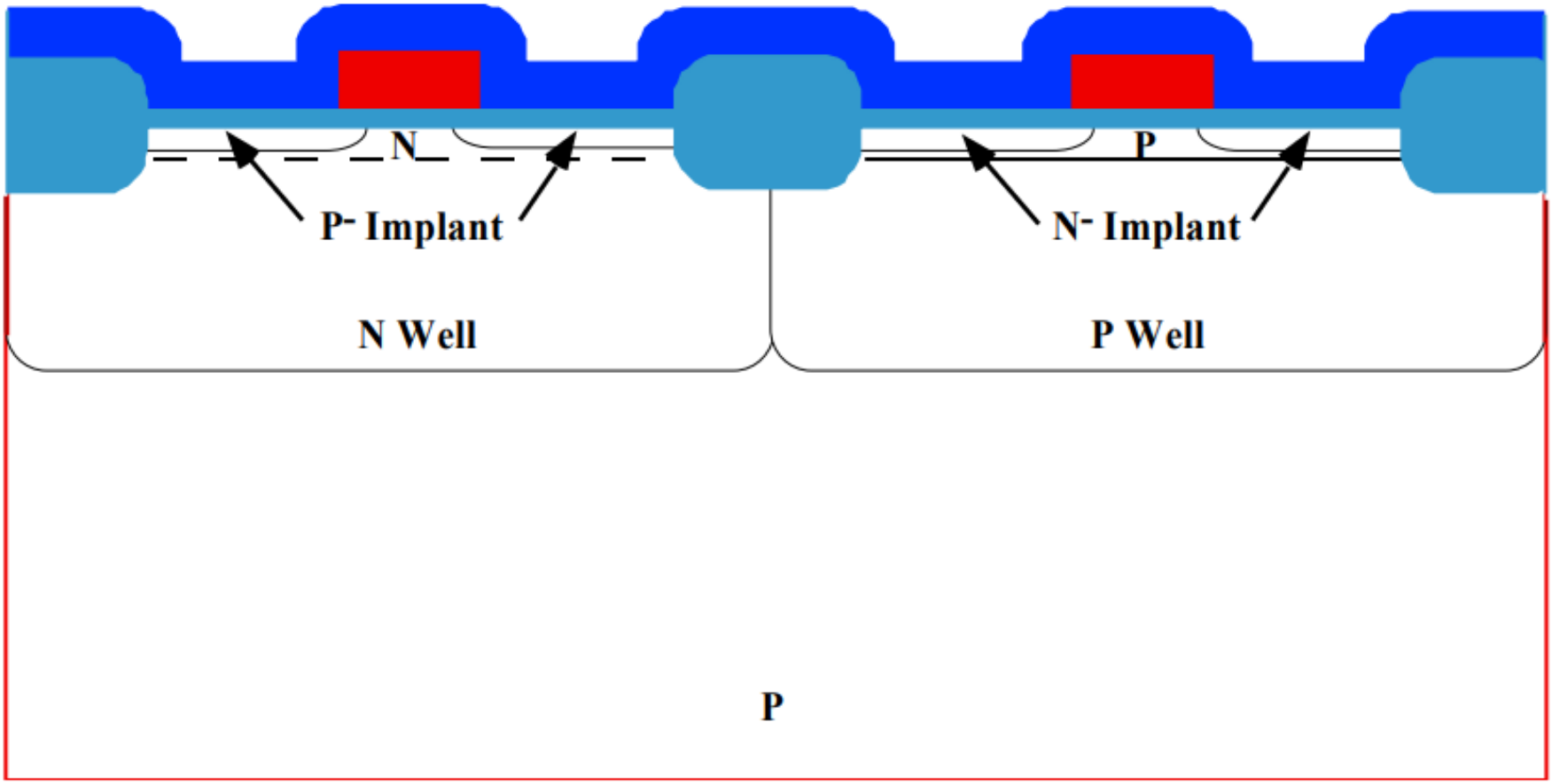
Mask #7 protects the PMOS devices. A P^+ implant forms the LDD regions in the NMOS devices (typically 5 x 10^{13} cm^{-2} @ 50 KeV).



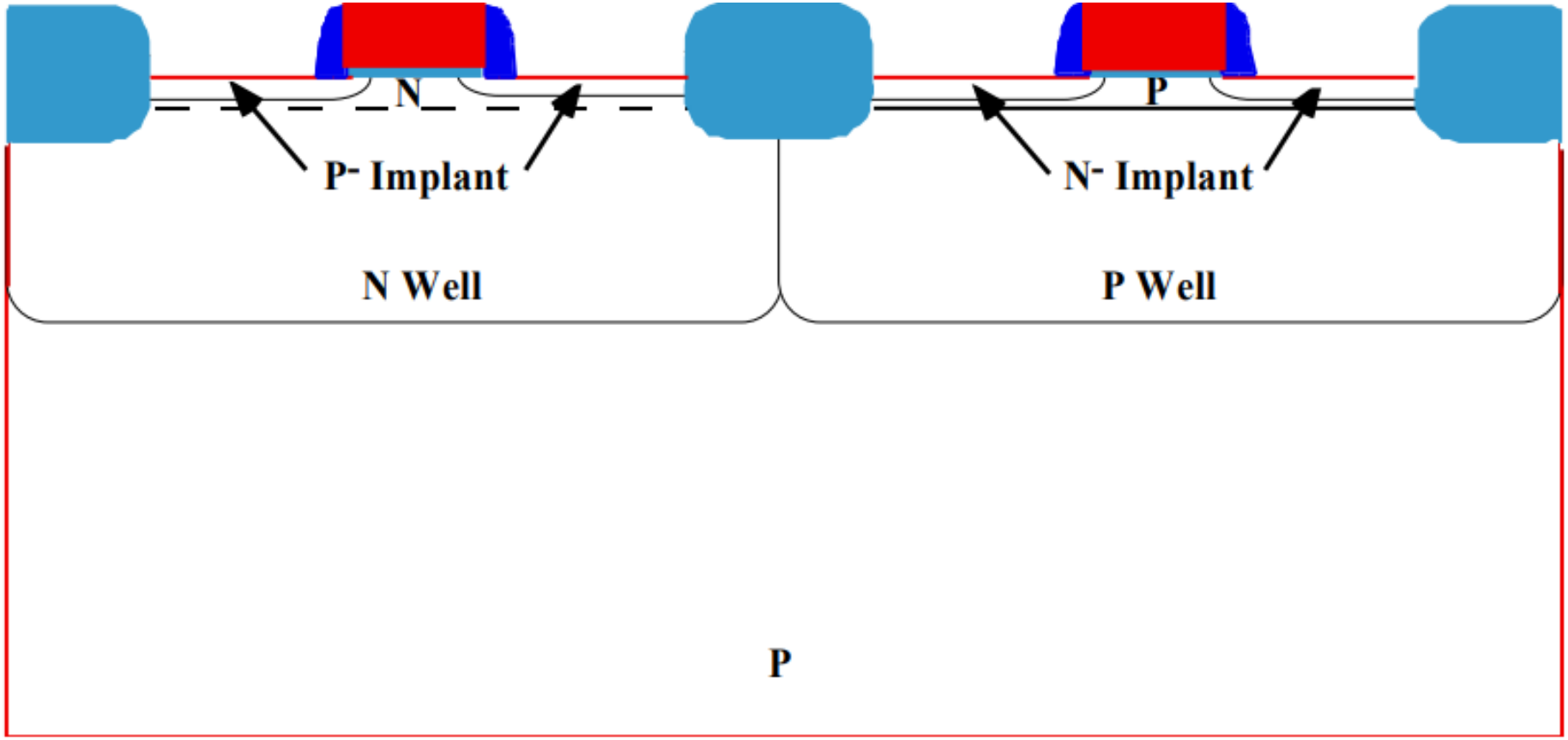
Mask #8 protects the NMOS devices. A B^+ implant forms the LDD regions in the PMOS devices (typically 5 x 10^{13} cm^{-2} @ 50 KeV).



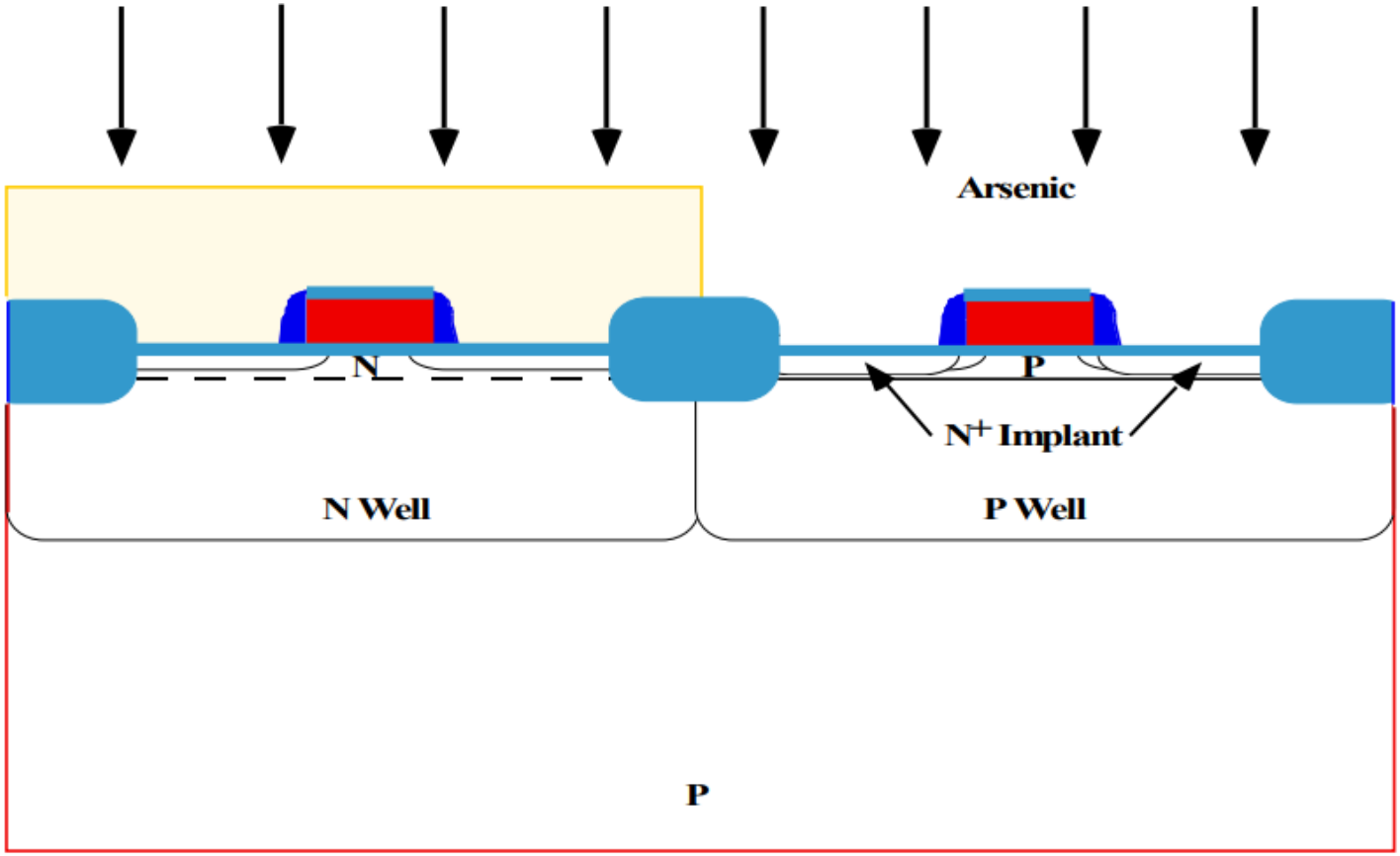
Conformal layer of SiO_2 is deposited (typically 0.5 µm).



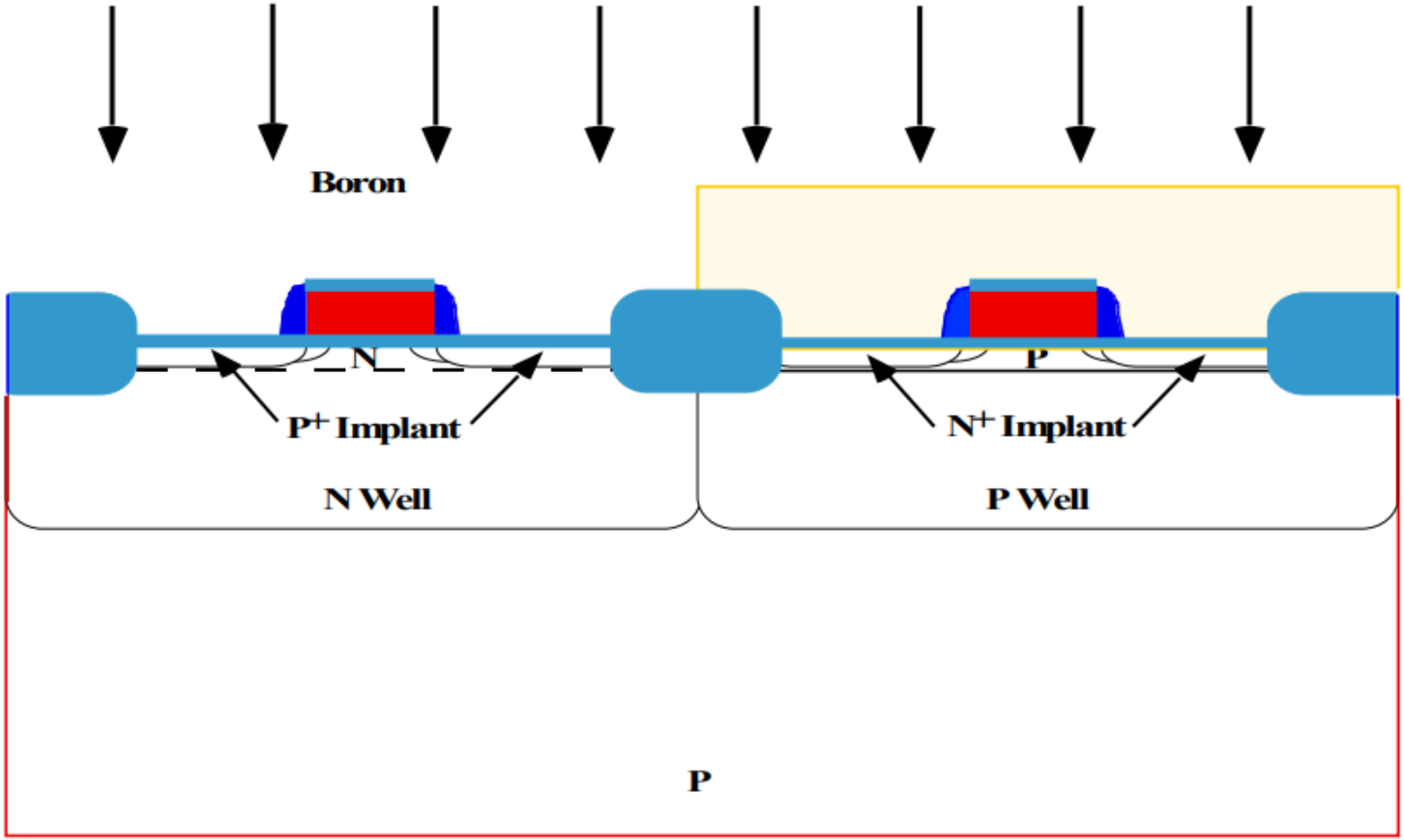
Anisotropic etching leaves “sidewall spacers” along the edges of the poly gates.



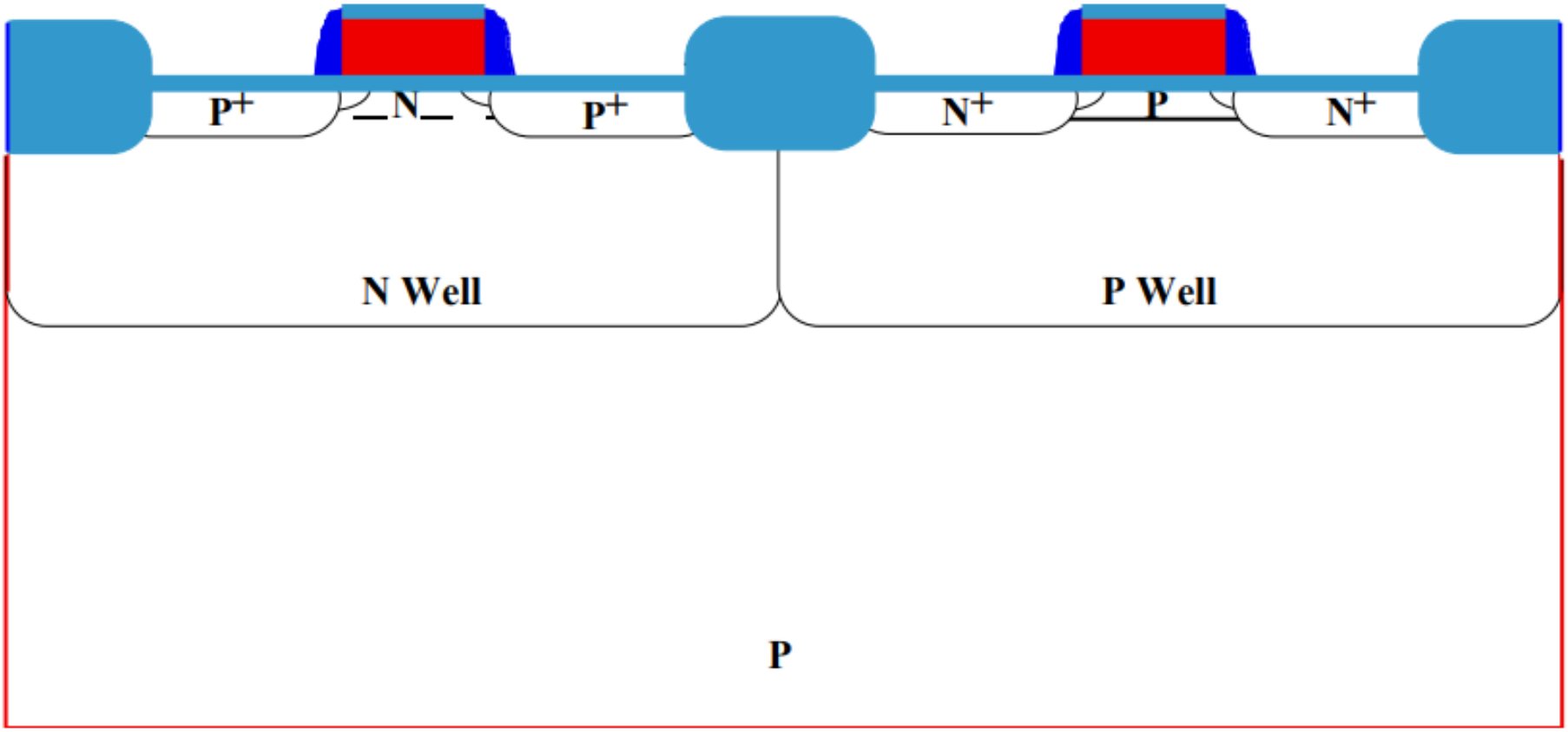
Mask #9 protects the PMOS devices, An As^+ implant forms the NMOS source and drain regions (typically 2-4 x 10^{15} cm^{-2} @ 75 KeV).



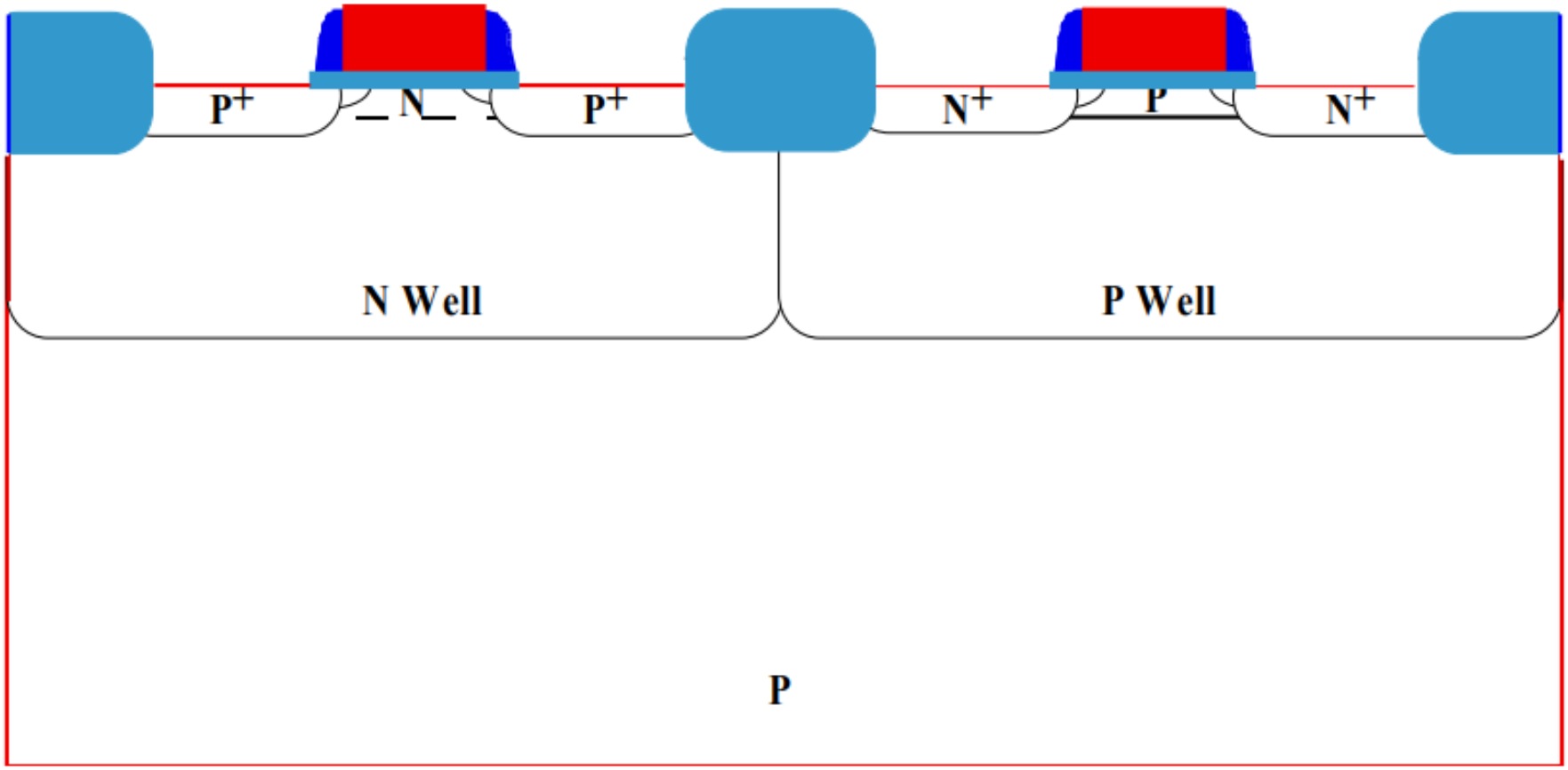
Mask #10 protects the NMOS devices, A B^+ implant forms the PMOS source and drain regions (typically 1-3 x 10^{15} cm^{-2} @ 50 KeV).



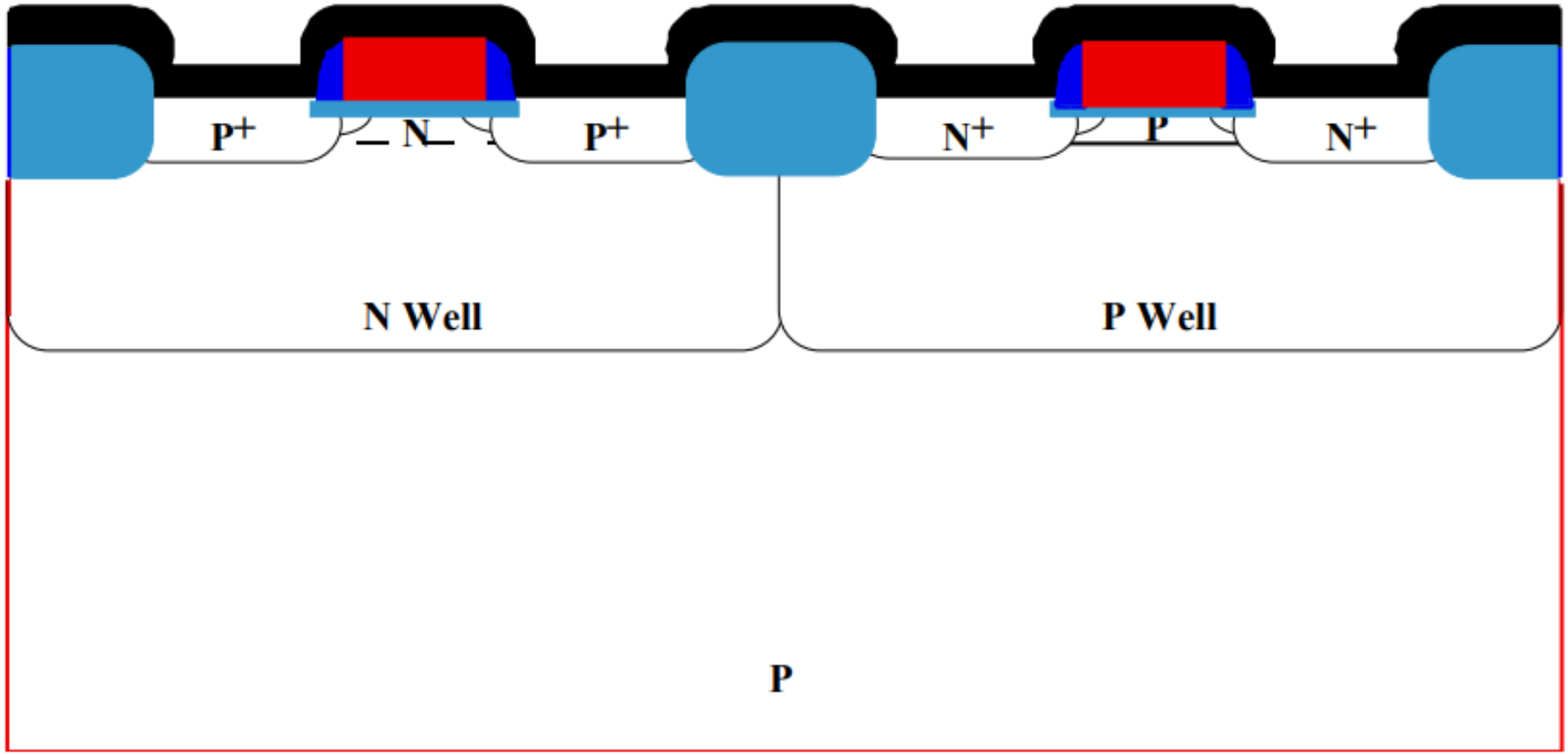
A final high temperature anneal drives-in the junctions and repairs implant damage (typically 30 min @ 900˚C or 1 min @ 1000˚C.



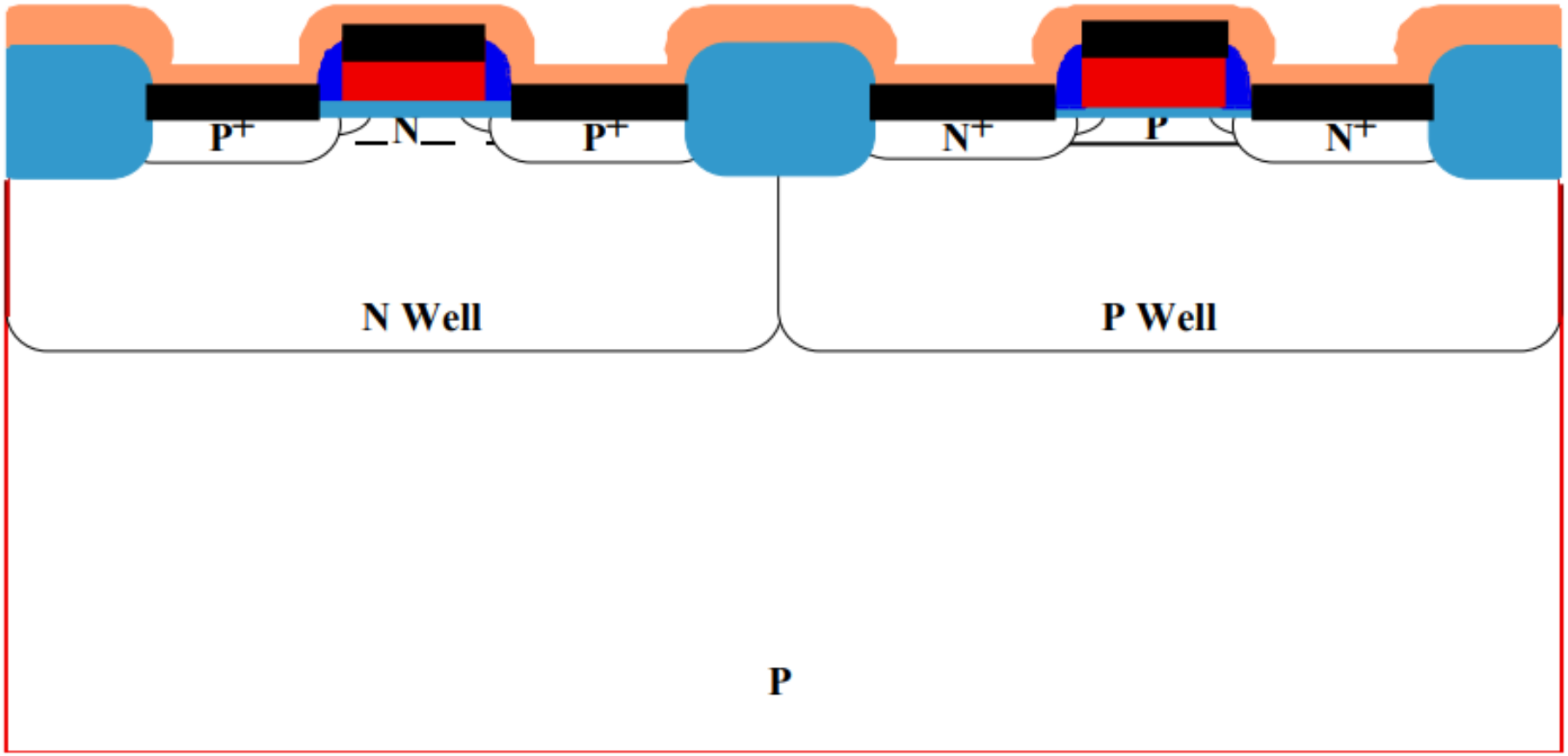
An unmasked oxide etch allows contacts to Si and poly regions.



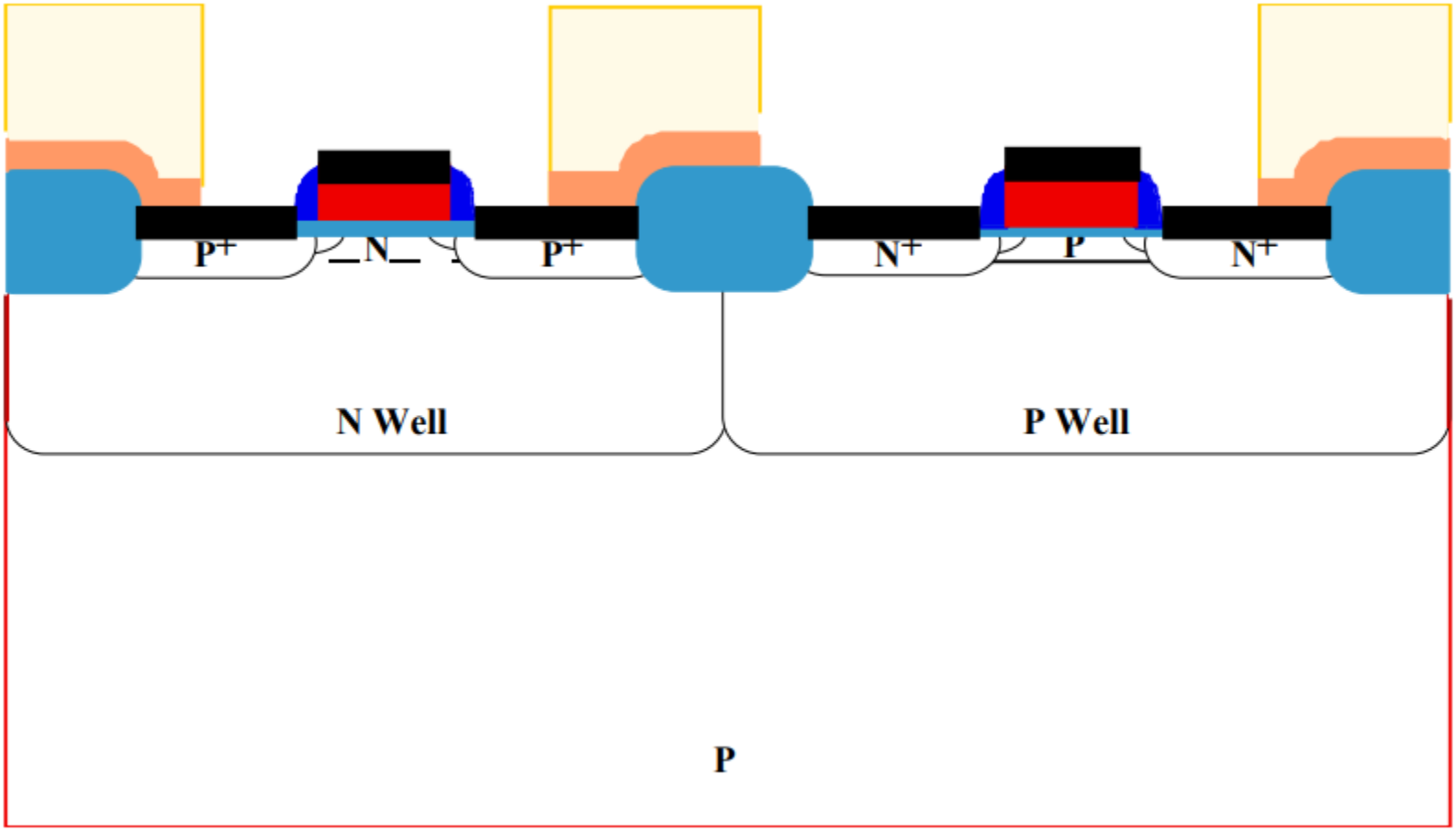
Ti is deposited by sputtering (typically 100 nm).



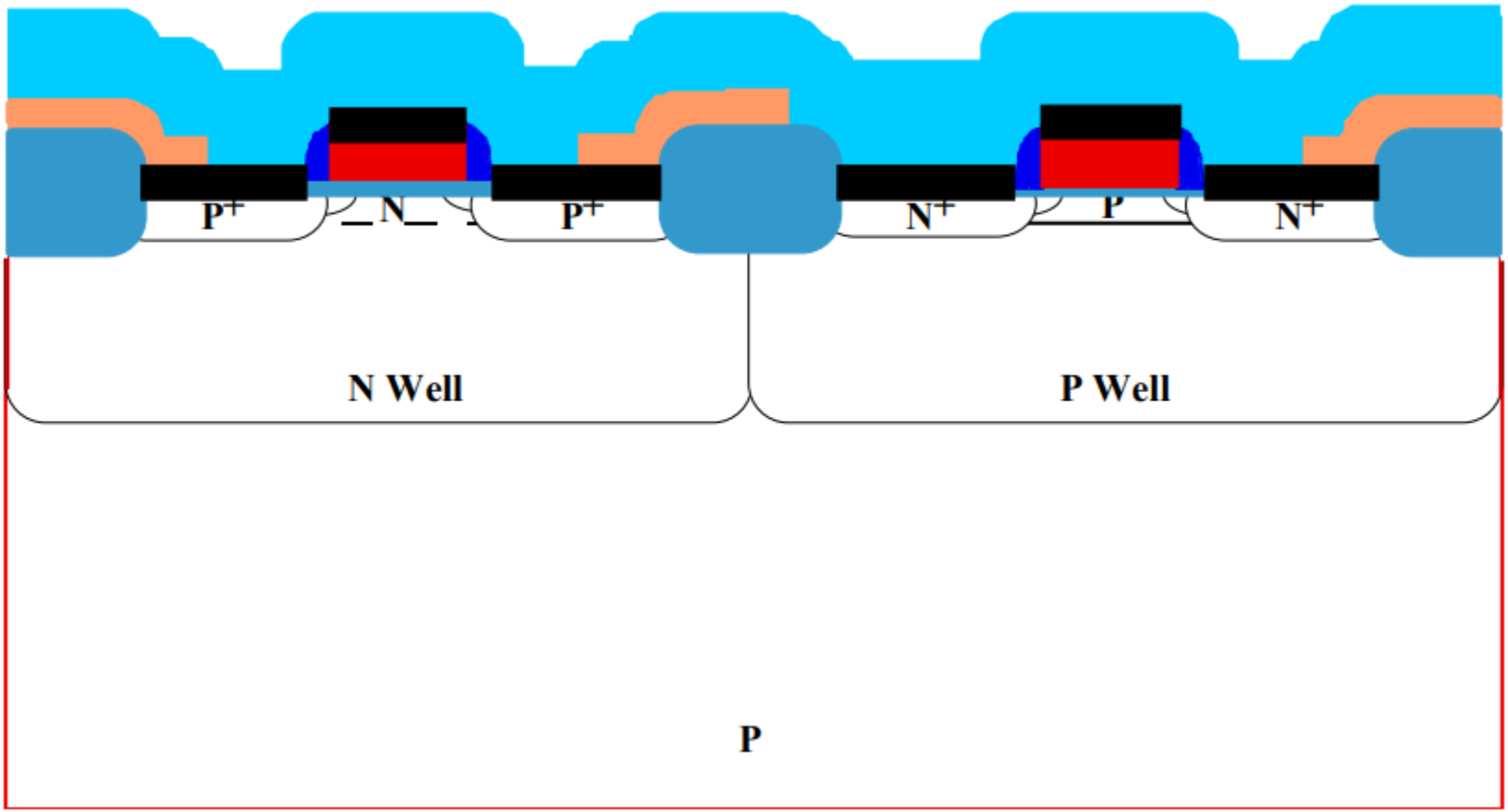
The Ti is reacted in an N_2 ambient, forming $TiSi_2$ and TiN (typically 1 min @ 600 - 700 ˚C).



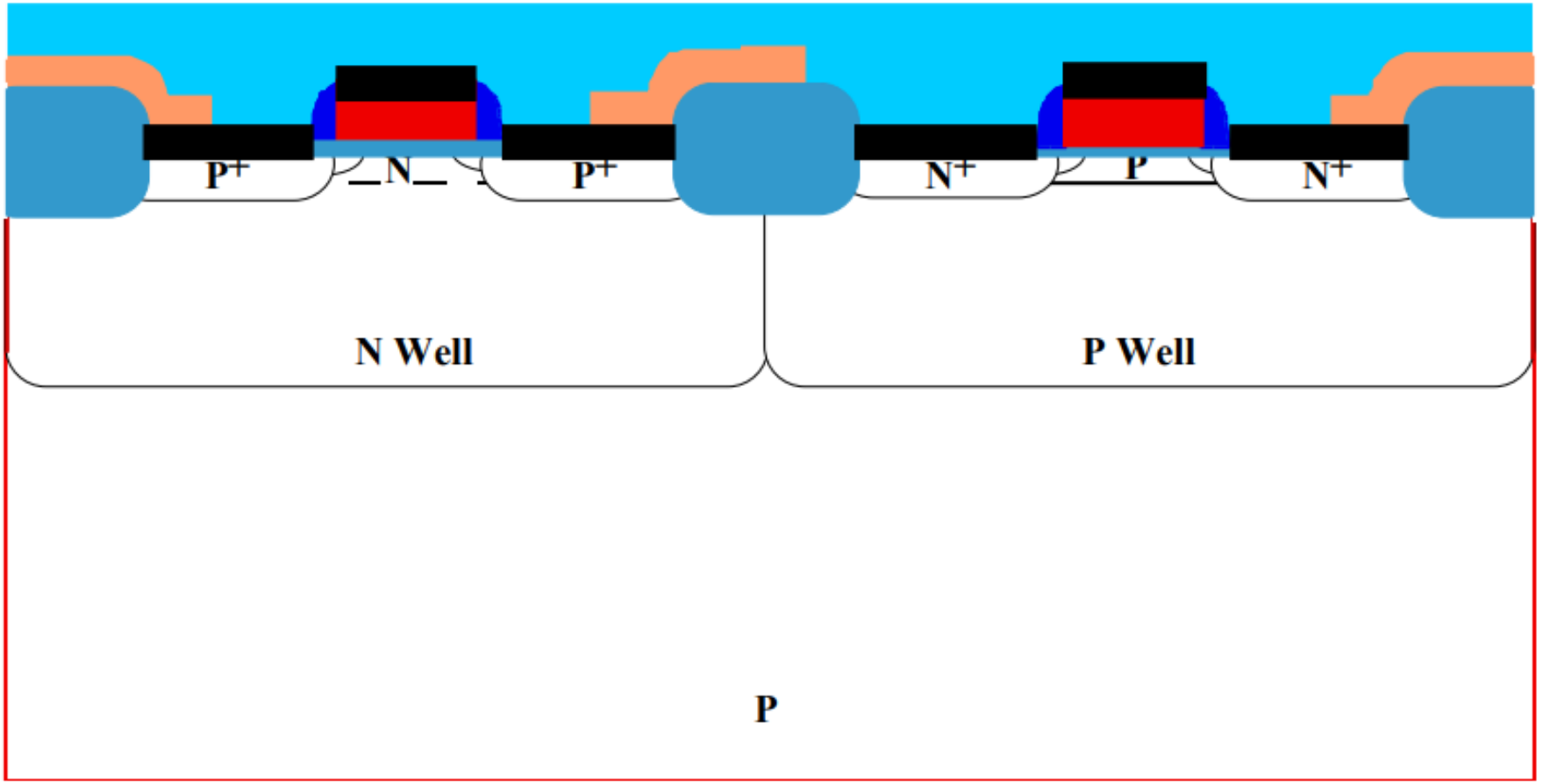
Mask #11 is used to etch the TiN, forming local interconnects.



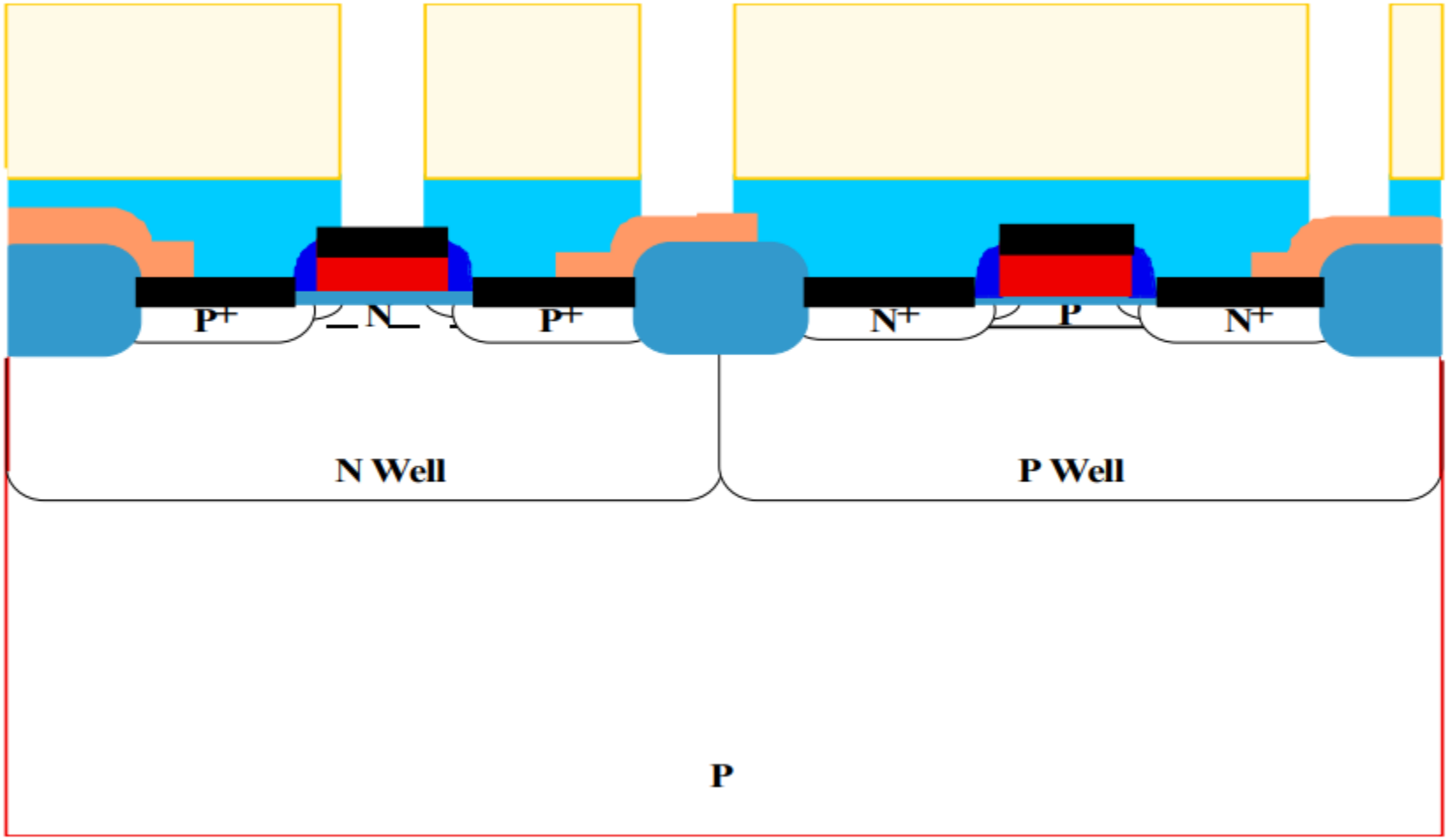
A conformal layer of SiO_2 is deposited by LPCVD (typically 1 µm).



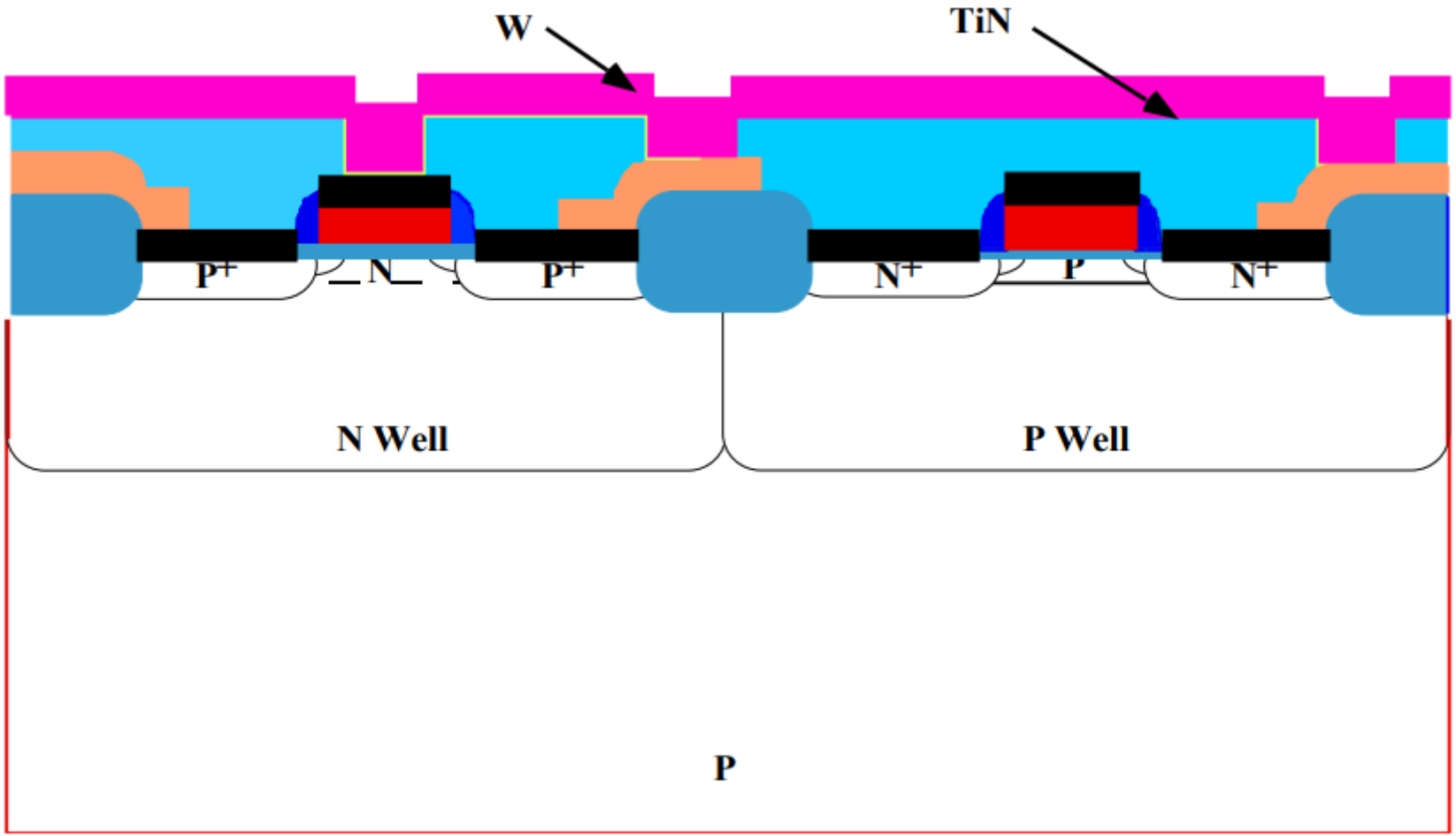
CMP is used to planarize the wafer surface.



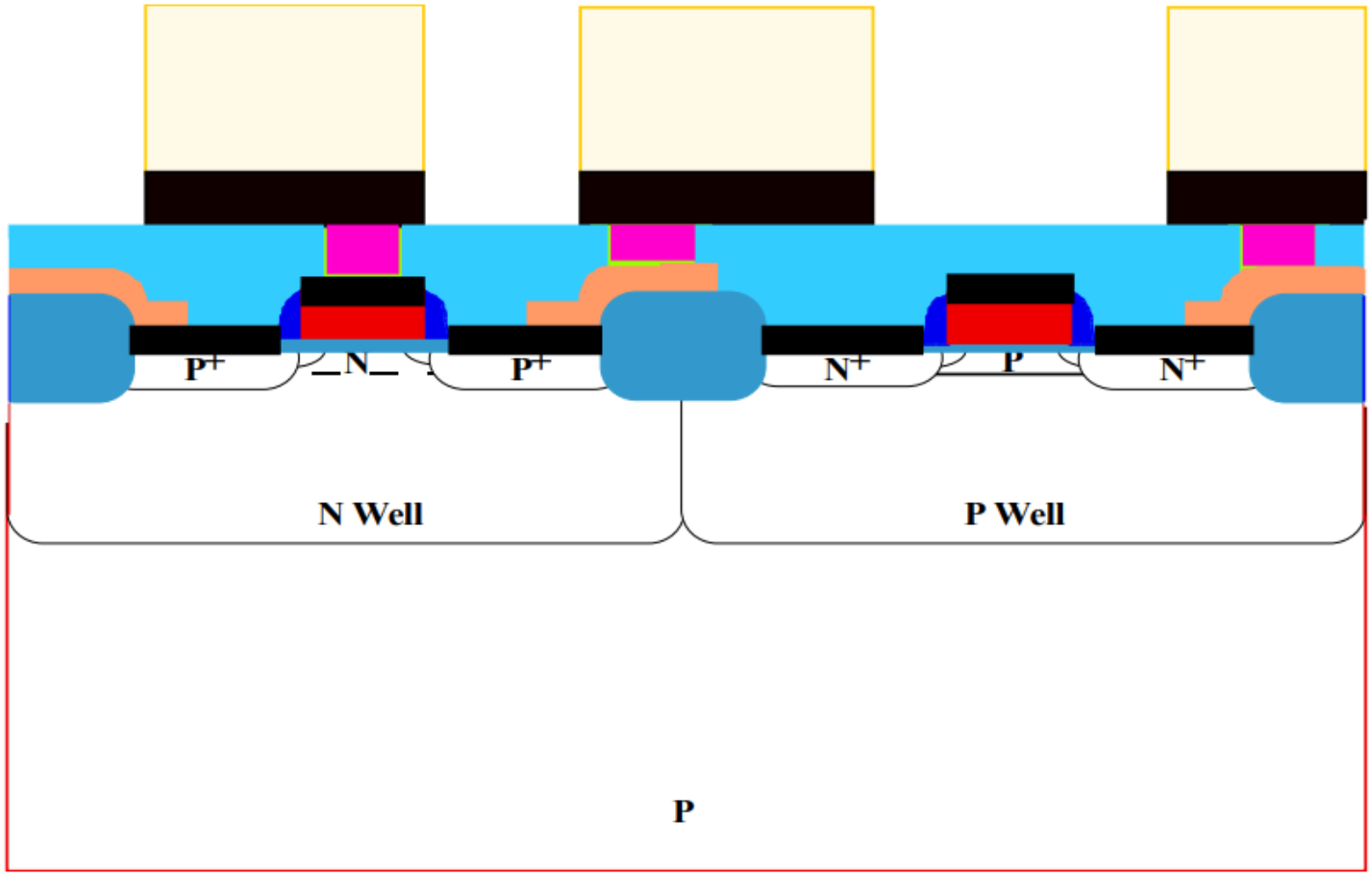
Mask #12 is used to define the contact holes. The SiO_2 is etched.



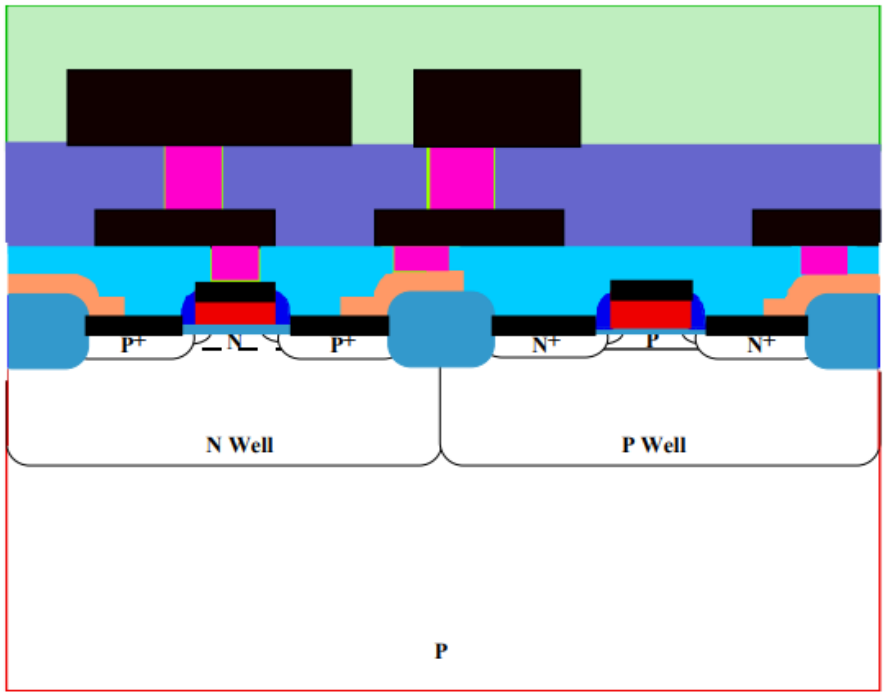
A thin TiN barrier layer is deposited by sputtering (typically a few tens of nm). followed by W CVD deposition.



Al is deposited on the wafer by sputtering. Mask #13 is used to pattern the Al and plasma etching is used to etch it.



Intermetal dielectric and second level metal are deposited and defined in the same way as level #1. Mask #14 is used to define contact vias and Mask #15 is used to define metal 2. A final passivation layer of Si_3N_4 is deposited by PECVD and patterned with Mask #16.



Budapest University of Technology and Economic
Department of Electron Devices

Circuit Environment

Lecture 4

Introduction to the Integrated Circuits Packaging

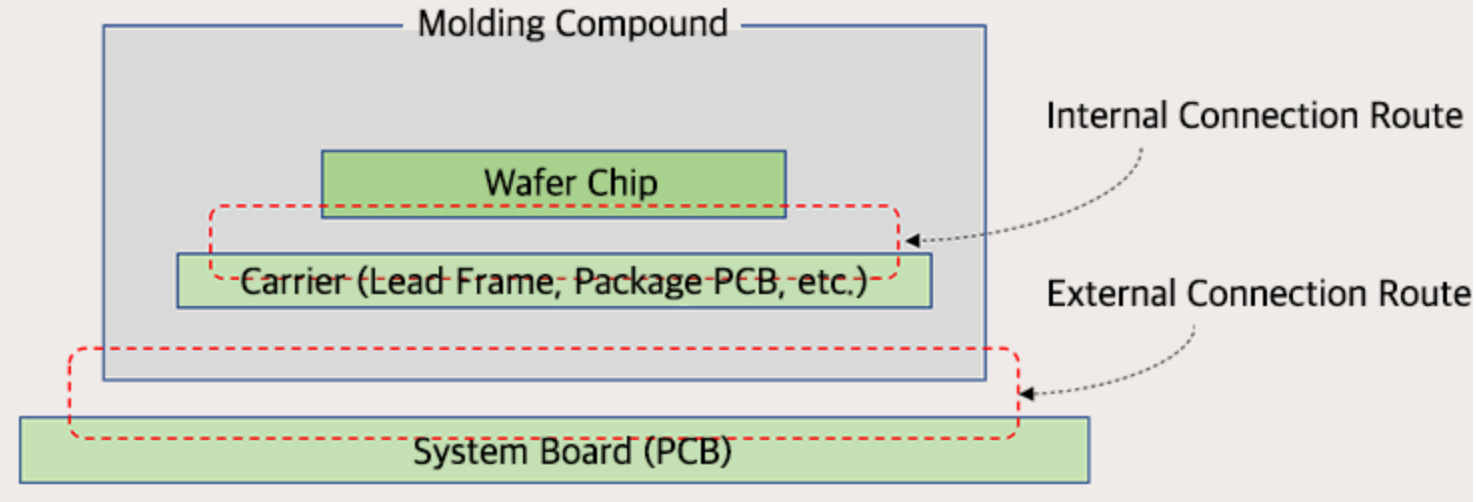
Packaging Definition

- Integrated circuit packaging is the final stage of semiconductor device fabrication, in which the block of semiconductor material is encapsulated in a supporting case that prevents physical damage and corrosion.

- The case, known as a "package", also supports the electrical contacts which connect the device to a circuit board.

- In the integrated circuit industry, the process is often referred to as packaging. Other names include semiconductor device assembly, assembly, encapsulation or sealing.

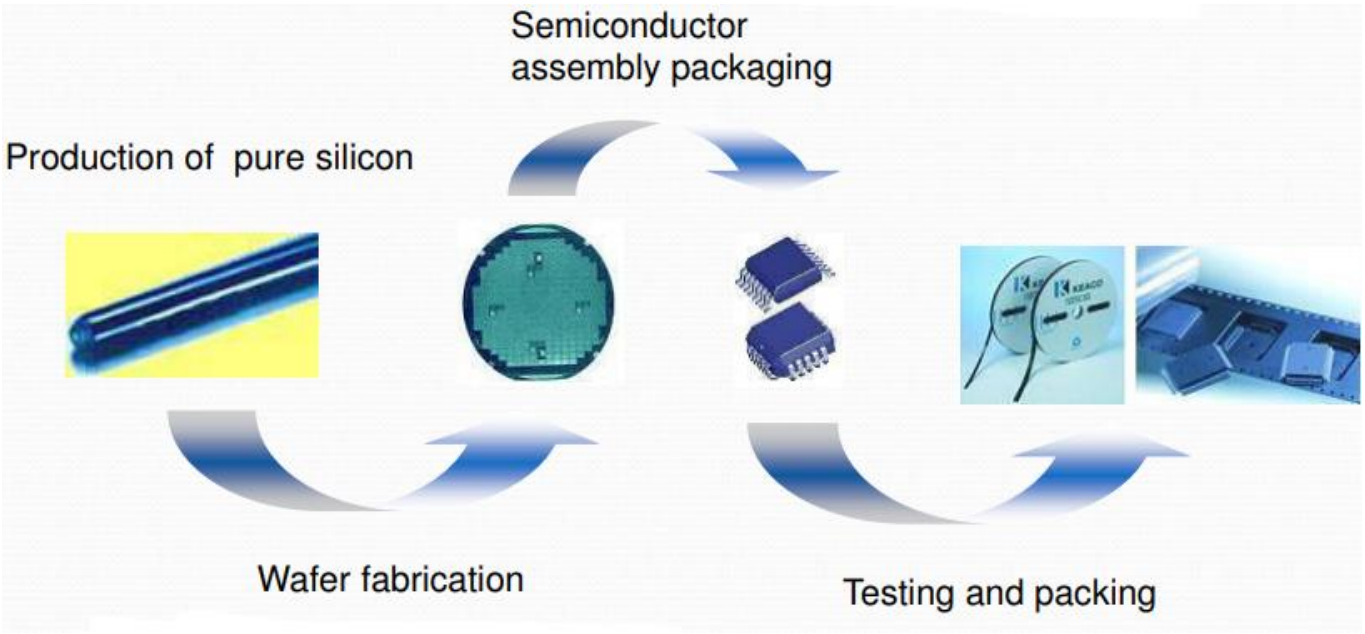
- The semiconductor packaging consists of a semiconductor chip, a carrier (package PCB, lead frame, etc.) on which the chip is placed, and a molding compound which surrounds them.



- The internal and external connection were previously made with lines (wires or lead frames). Recently, points (bumpers or balls) are typically being used.

- Meanwhile, molding compounds play an important role in taking out the heat inside and protecting the chip from external damage.

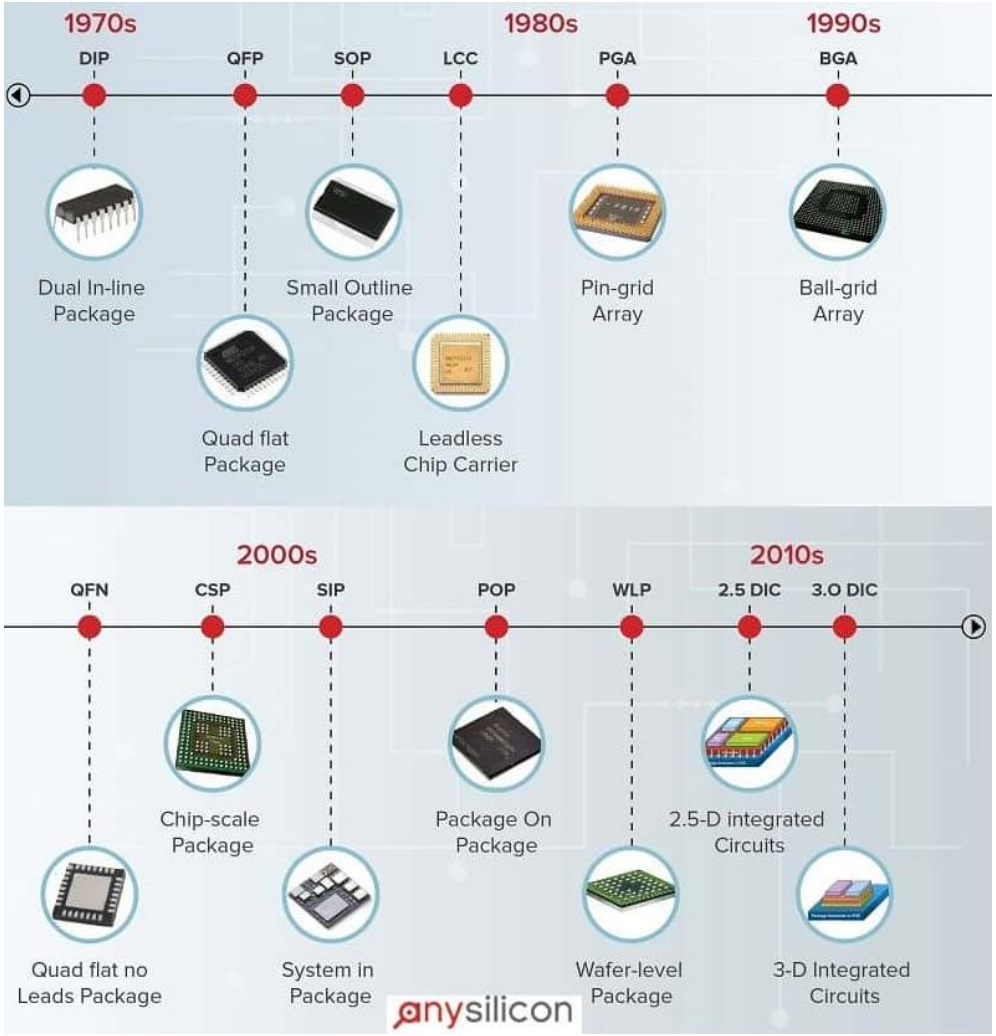
- The packaging stage is followed by testing of the integrated circuit.



Needs of Packaging

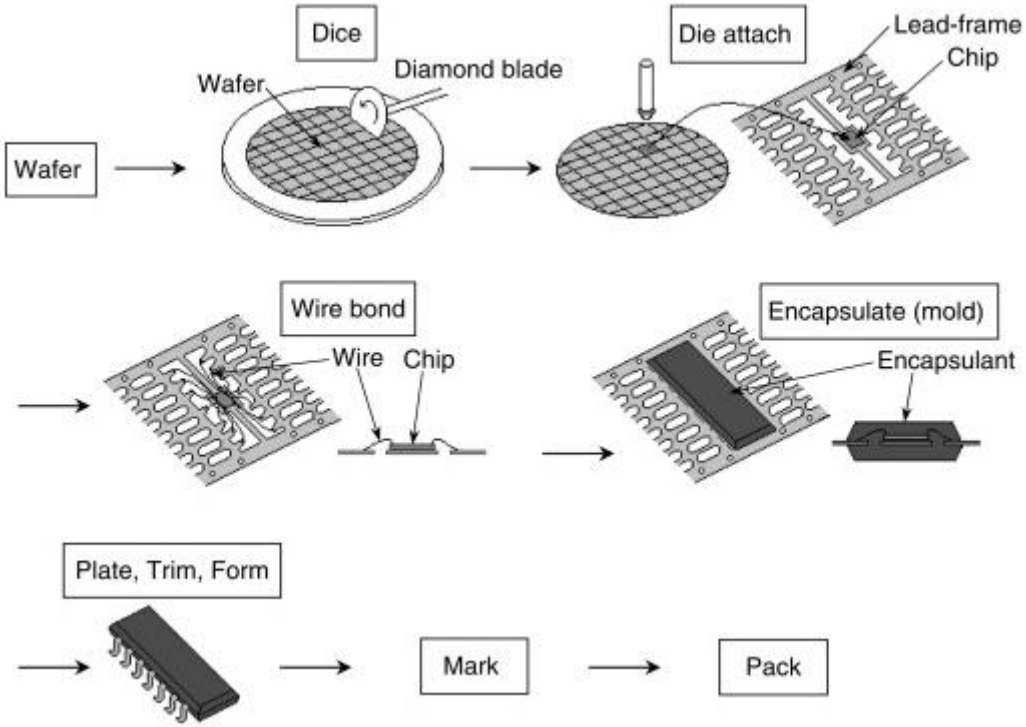
- The IC packaging has many functions. These functions include:
  - Environmental protection is needed to prevent chemical damage that would be detrimental to the IC performance.
  - Mechanical stability and thermal management are both required to increase the reliability and lifetime of the IC by preventing physical damage.
  - Electrical connections must be made between the package and the IC to enable interaction with a larger system on a circuit board.

Packaging History



IC Packaging Phases

- The main operations performed are Die attaching, IC bonding , and IC encapsulation.

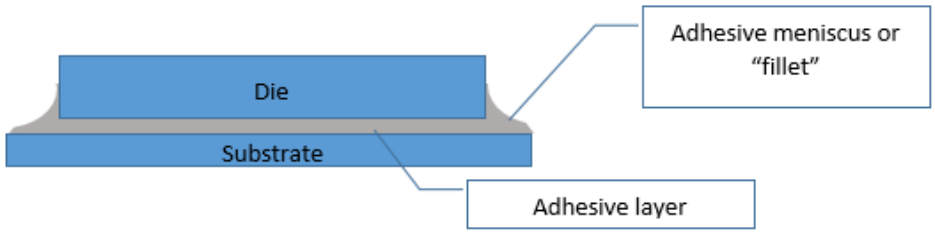


1. Die attachment

- Die attachment is the process of attaching the silicon chip to the die pad or die cavity of the support structure (e.g. lead frame) of the semiconductor package.
- There are two common die attach processes
  - Adhesive die attach

➢ It uses adhesives such as **polyimide**, **epoxy** and **silver-filled glass** as die attach material to mount the die on the die pad or cavity.

➢The mass of epoxy climbing the edges of the die is known as the die attach fillet. Excessive die attach fillet may lead to die attach contamination of the die surface. Too little of it may lead to die lifting or die cracking.



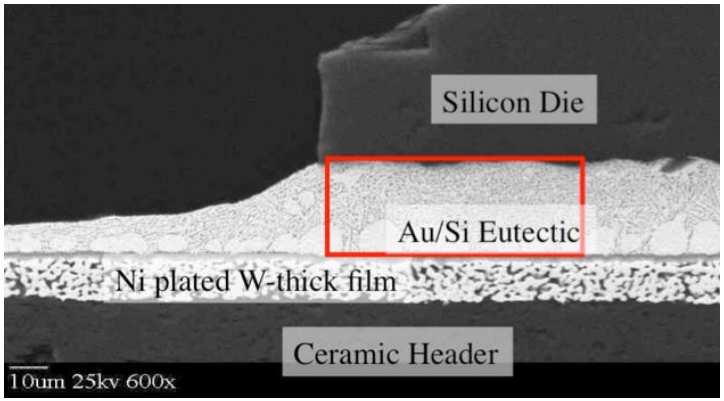
➢ Die attach films or tapes can also be employed instead of adhesives but they are less easy to apply and requiring more substantial equipment expenditure.

➢UV adhesives offer another method of attaching dies but due to shadow areas underneath the die or wafer can't be cured with UV light alone, a secondary cure method such as a thermal cure is required.

- Eutectic die attach.

➢ It uses a **eutectic alloy** to attach the die to the cavity. A eutectic alloy is an alloy with the lowest melting point possible for the metals combined in the alloy.

➢The Au-Si eutectic alloy is the most used die attach alloy in semiconductor packaging.



- Both processes use special die attach equipment and die attach tools to mount the die.
- The presence of voids in the die attach material affects the quality and reliability of the device itself.
- Large die attach voids result in low shear strength and low thermal/electrical conductivity and produce large die stresses that may lead to die cracking.
- Small voids provide sufficient shear strength and electrical/thermal conductivity, while 'cushioning' large dice from stresses.
- Total absence of voids may mean high strength, but it may also induce large dice to crack. The strength of die attachment is measured using the die shear test.

2. Wire Bonding

- Wire bonding, is the process of providing electrical connection between the silicon chip and the external leads of the semiconductor device using very fine bonding wires.

- The wire used in wire bonding is usually made either of gold (Au) or aluminium (Al), although Cu wire bonding is starting to gain a foothold in the semiconductor manufacturing industry.

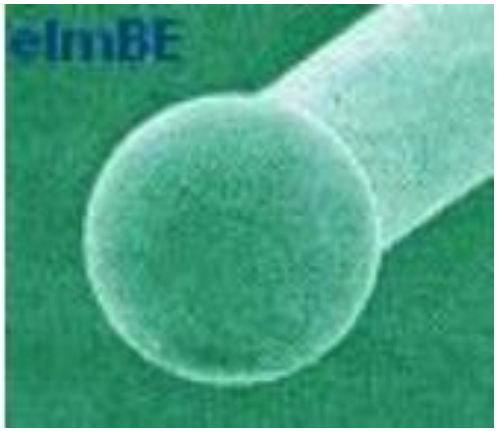
- There are two common wire bonding processes

  - Au ball bonding

  - Al wedge bonding

- Au ball bonding

  - A gold ball is first formed by melting the end of the wire through electronic flame-off process (EFO).



  - This free-air ball has a diameter ranging from 1.5 to 2.5 times the wire diameter. Free air ball size consistency, controlled by the EFO, and the tail length is critical in good bonding.

  - Adequate amounts of pressure, heat, and ultrasonic forces are then applied to the ball for a specific amount of time, forming the initial metallurgical weld between the ball and the bond pad.

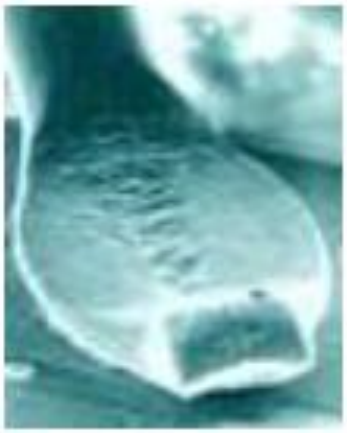
- The wire is then run to the corresponding finger of the leadframe, forming a gradual arc or "loop" between the bond pad and the leadfinger.

- Pressure and ultrasonic forces are applied to the wire to form the second bond (known as a wedge bond.

- Al wedge bonding

  - A clamped aluminium wire is brought in contact with the aluminium bond pad.

  - Ultrasonic energy is then applied to the wire for a specific duration while being held down by a specific amount of force, forming the first wedge bond between the wire and the bond pad.



  - The wire is then run to the corresponding lead finger, against which it is again pressed.

  - The second bond is again formed by applying ultrasonic energy to the wire. The wire is then broken off by clamping and movement of the wire.

- Gold ball bonding is much faster than aluminum wedge bonding, which is why it is extensively used in plastic packaging.

- Unfortunately, gold ball bonding on Al bond pads can not be used in hermetic packages, primarily because the high sealing temperatures (400-450 deg C) used for these packages tremendously accelerate the formation of Au-Al intermetallic that can lead to early life failures

3. IC Encapsulation

- After wire bonding, it is important to protect the IC package by applying molded encapsulation.

- Encapsulation provides an economical way to protect device packages by:
  - Isolating the active devices from environmental pollutants.
  - Offering mechanical protection.

- A commonly used process is **transfer molding**, in which high temperature and pressure forced through a mold chase over the die and die frame and into the cavity on the frame where the die was placed earlier. The hardened epoxy forms the body of the final package.

- Controlling time, pressure, and flow are critical issues in the encapsulation step.

- Miscalculations can cause several problems such as wire sweep (wires pushed together causing a short circuit within the component), or partial molding and mold voiding, which are pockets (or bubbles) that form in the mold during the process.

- Another die-protecting option is ceramic packaging. In ceramic packages, instead of a molded cover, a cap of either ceramic or metal is welded or sealed over the die, encasing it in a sealed environment.

Package Type & Trend

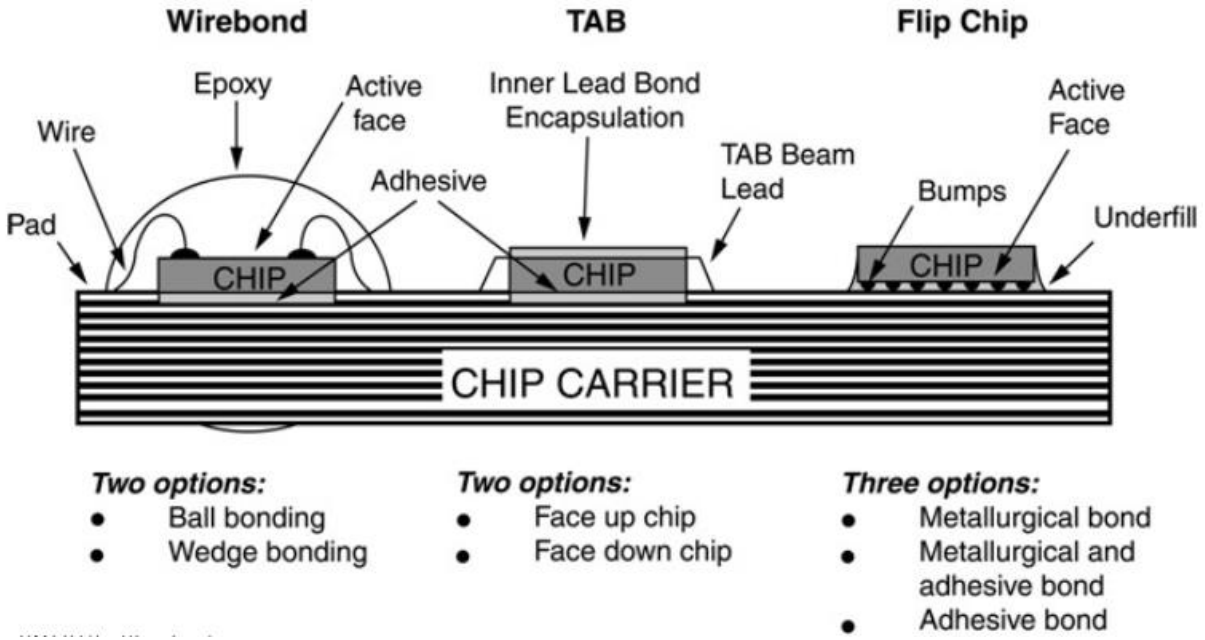
Packages being categorized in few ways

- Type of substrate used
- Chip configuration / arrangement
- Type of interconnection
- Type of protection
- Package grouping based on its characteristic
- Type of board mounting
- Type of electronic packaging levels

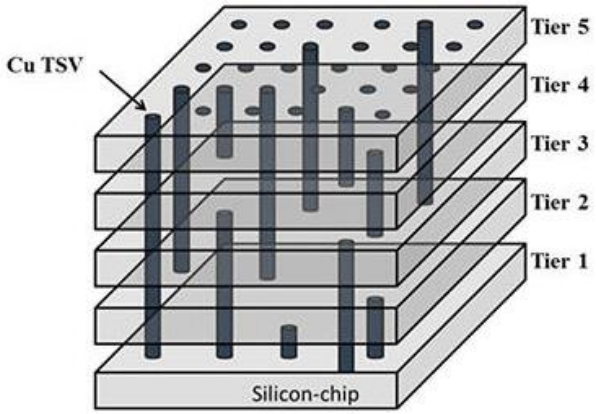
- Type of substrate used

  - Metal Can, Lead frame, Ceramic, PCB , Flexible / laminated / tape and Bare die

- Type of interconnection (The process of creating the interconnection between the die of an IC with lead).
  - Wire bonding
  - Bridge
  - Tape Automated Bonding (TAB)
  - Flip chip
  - Direct Chip Attachment (DCA)



- Through-silicon via (TSV)
  - Its is a vertical electrical connection that passes completely through a silicon wafer or die.
  - TSVs are high-performance interconnect techniques used as an alternative to wire-bond and flip chips to create 3D packages and 3D integrated circuits.

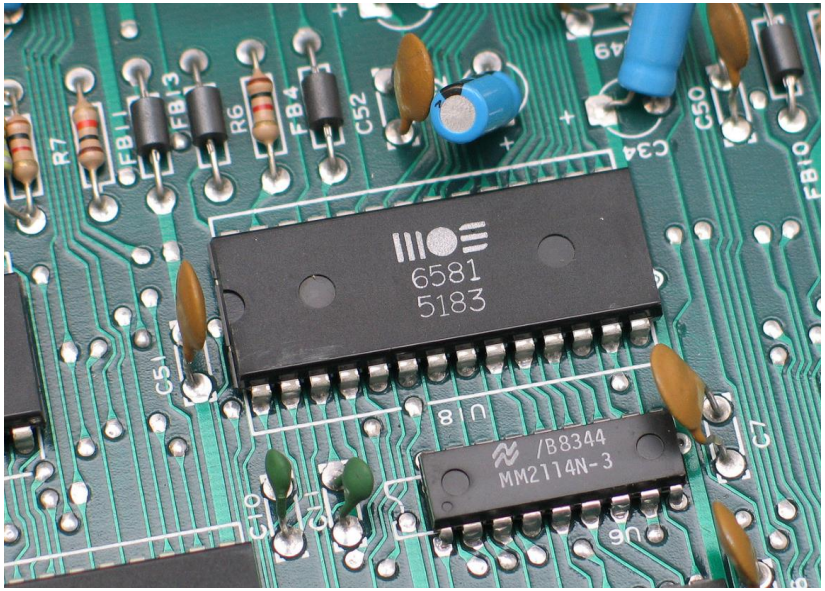


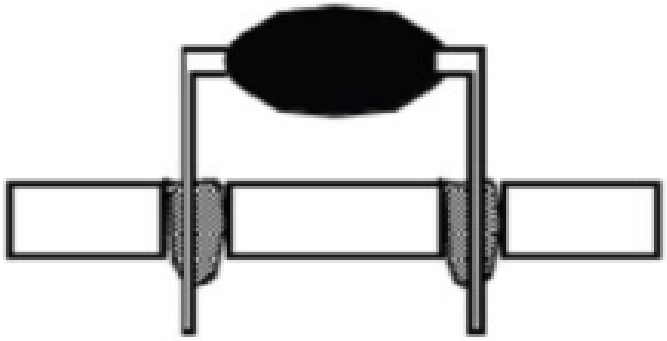
- Type of protection
  - Metal Can
  - Plastic/Ceramic Covered
  - Singulated Molding
  - Mold array process MAP
  - Wafer level

- Package grouping based on its characteristic
  - Optical
  - Sensor
  - I/O Card
  - Hermetic
- Type of board mounting
  - Through-Hole Mount Packages
  - Surface Mount Packaging

Through-Hole Mount Packages

- They are designed in a way that the lead pins are stuck through one side of the board and soldered on the other.





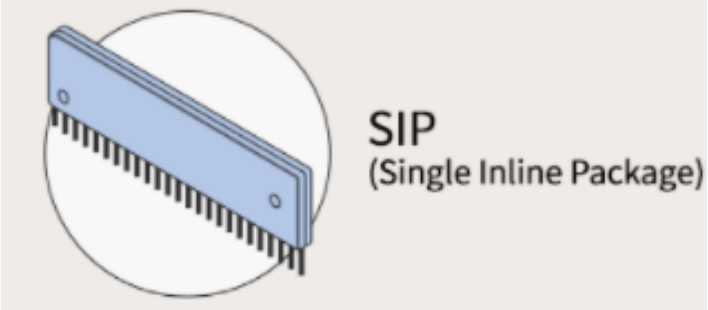
- They are bigger in size as compared to the other kind. These are majorly used in electronic equipment to compensate for the board space and cost limitations.

- Through-hole mount packages come in ceramic and plastic types. The package varies in size due to the difference in the number of pins in different packages.

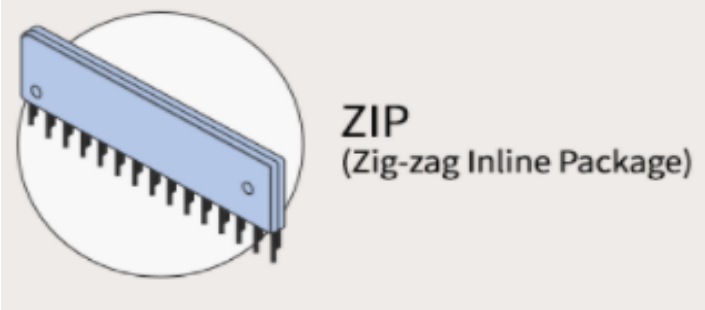
- These pins are placed in a manner that they can be adjusted on to the centre of a breadboard without short-circuiting each other or even get soldered into PCBs.

Through-Hole Mount Package types

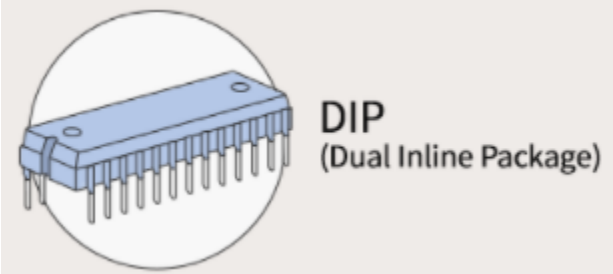
- A Single Inline Package (SIP) is a computer chip package that contains only a single row of connection pins.



- Zig-zag Inline Package (ZIP) was a short-lived packaging technology for integrated circuits, particularly dynamic RAM chips. It was intended as a replacement for Dual Inline Package (DIP).

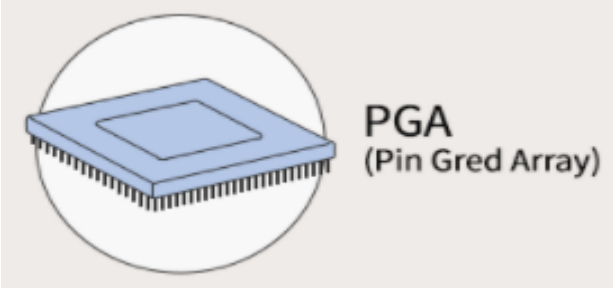


- Dual Inline Package (DIP) is an electronic component package with a rectangular housing and two parallel rows of electrical connecting pins.



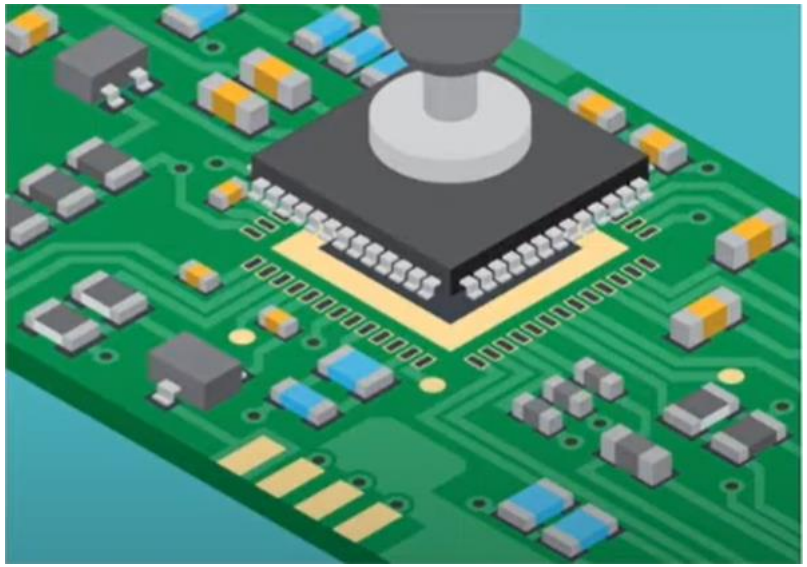
  - There are many types of DIP Packages, Plastic Dual In-Line Package (PDIP) and Molded Dual In-Line Package (MDIP) are the few popular types.

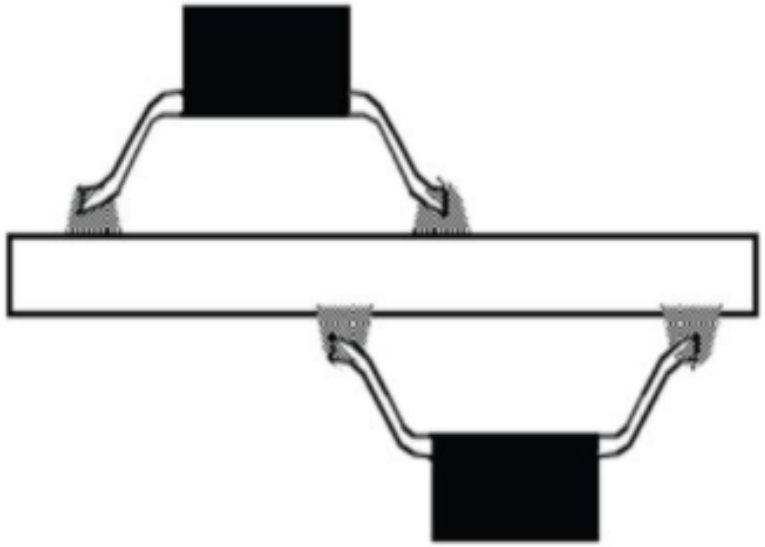
- Pin Grid Array (PGA) is square or rectangular, and the pins are arranged in a regular array on the underside of the package.



Surface Mount Packaging

- The leads do not pass-through holes in the PCB. Instead, surface mount package leads are aligned to electrical contacts on the PCB and are connected simultaneously by solder reflow.





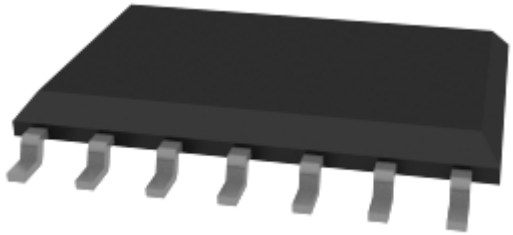
- Surface mount packaging follows the technology of mounting or placing the components directly on the printed circuit board surface. Although this process of fabrication helps do things quickly, it also increases the chances of defects.

- This is because of the miniaturization of components and also because they are mounted extremely close to each other.

- This, in turn, results in making it extremely important to detect the failure in the entire process. Again, Surface mount packaging also uses ceramic or plastic molding.

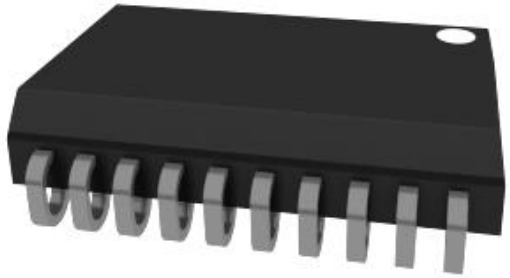
- **Surface Mount Package types**
  - Single Side
    - Surface Vertical-Mount (SVP)

  - Dual Side
    - Small Outline Package (SOP) packages are characterized by gull-wing type leads are drawn from each package body in two directions and can be mounted flat.

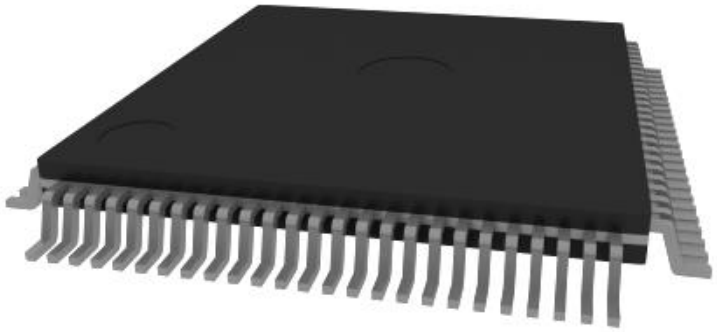


- Thin-Small Outline Package (TSOP). They are very low-profile (about 1 mm) and have tight lead spacing (as low as 0.5 mm).

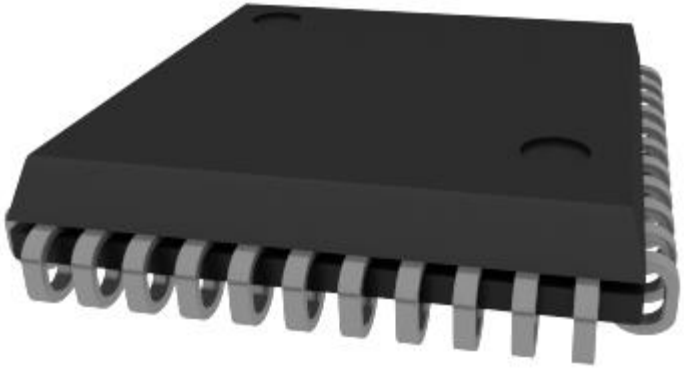
- Small Outline J-lead Package (SOJ) is a version of SOP with J-type leads instead of gull-wing leads.



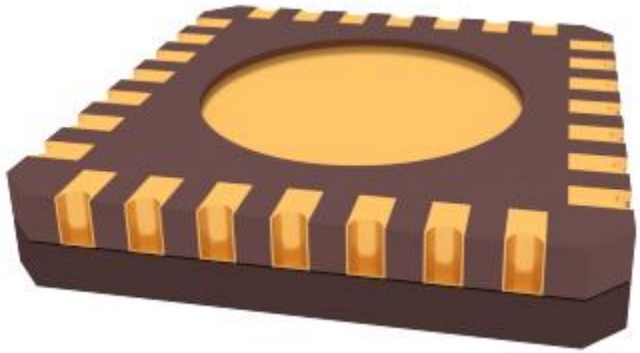
- Quadruple Side
  - Quad Flat Package (QFP) is a surface mount integrated circuit package with “gull wing” leads extending from each of the four sides.



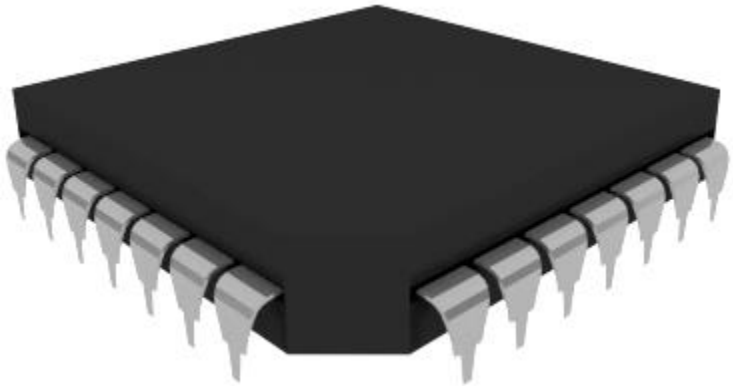
  - Quad Flat J-lead Package (QFJ) are characterized by J-shaped leads which are drawn out from each package body in four directions and can be mounted flat.



- Leadless Chip Carrier (LCC) has no “leads”, but instead has rounded pins through the edges of the ceramic or molded plastic package.

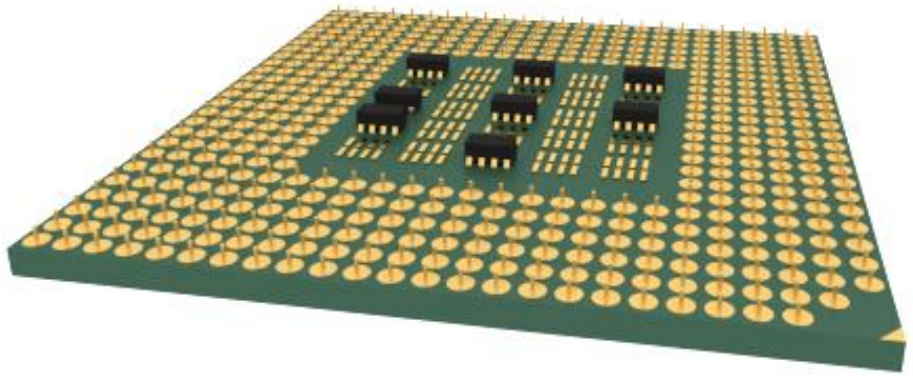


- Leadless Chip Carrier, Small Outline J-lead Package (LCC SOJ)



- Full Surface

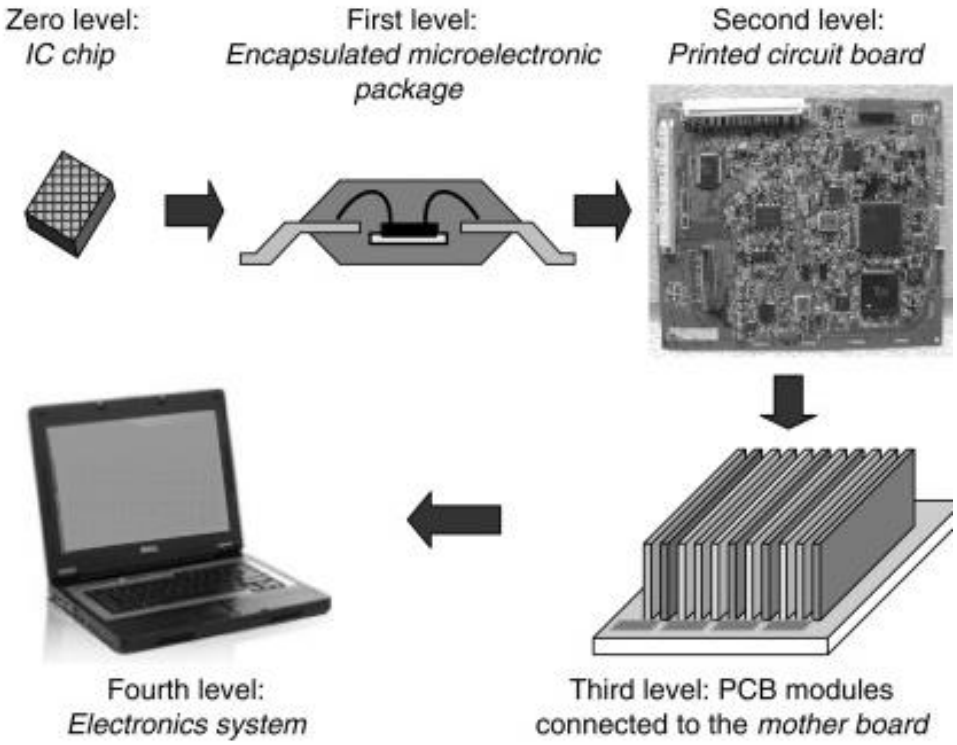
  - Ball Grid Array (BGA) is a type of surface-mount packaging (a chip carrier) used for integrated circuits. BGA packages are used to permanently mount devices such as microprocessors.



- Most packages can be made using ceramic or plastic. The integrated circuits are hermetically sealed for protection from the environment. The pins can be on one side (single inline or zigzag pattern of leads), two sides (dual inline package or DIP), or four sides of the package (quad package).

- Most advanced packages have leads distributed over a large portion of the surface of the package as in through-hole pin grid arrays (PGAs) or surface-mounted ball grid arrays (BGAs).

- Type of electronic packaging levels
  - The first-level packaging consists of the interconnection and encapsulation of the IC chip.
  - The second-level packaging consists of the connection of the microelectronic package to the PCB.



- PCBs may be further interconnected to a motherboard, known as third-level packaging.

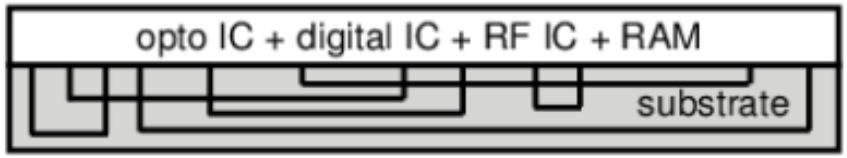
- The fourth and final packaging level is the packaging of the motherboard (or PCBs) in an electronic system such as a laptop computer or a cellular phone.

Chip configuration / arrangement

- Single chip (SCP)
  - Single chip package is a package that supports a single microelectronic device so that its electrical, mechanical, thermal, and chemical performance needs are adequately served

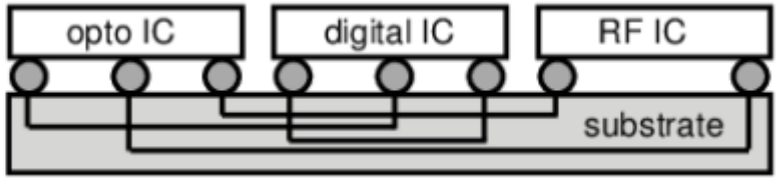
- System on chip (SOC)
  - It is an integrated circuit that integrates all or most components of a computer or other electronic system (CPU, memory, input/output ports and secondary storage) on a single substrate or microchip.

SOC
complete system
on one chip

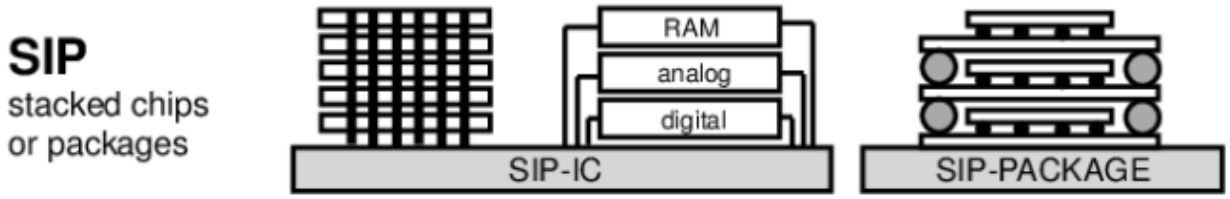


- Multi chip module (MCM)
  - An electronic assembly where multiple integrated circuits (ICs or "chips"), semiconductor dies and/or other discrete components are integrated, usually onto a unifying substrate.
  - Other terms for MCM packaging include "Heterogeneous integration" or "Hybrid Integrated Circuit"

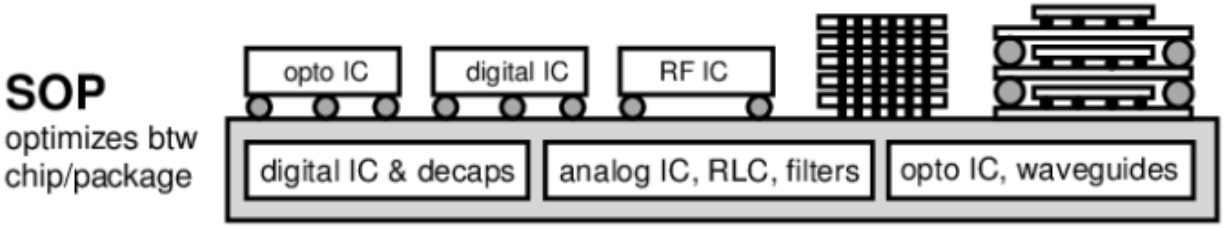
MCM
interconnects
components



- System in package (SIP)
  - It is a number of integrated circuits enclosed in one or more chip carrier packages that may be stacked using package on package.
  - The SIP performs all or most of the functions of an electronic system, and is typically used inside a mobile phone, digital music player, etc.
  - Dies containing integrated circuits may be stacked vertically on a substrate. They are internally connected by fine wires that are bonded to the package



- System on package (SOP)
  - It is an emerging system technology that goes beyond System-on-Chip (SOC) and System-in-Package (SIP) and forms the basis of all emerging digital convergent electronic and bioelectric systems.
  - Therefore, overcomes both the computing and integration limitations of SOC, SIP, MCM and traditional system packaging.



- Stacked chip
- Package interposer package (PiP)/ Package on package (PoP)
- 3D Packaging

- **Further, it can be classified as**

  - **Standard** - This is the most common packaging. The pins are spaced 0.1” apart.

    - DIP (Dual In-line Package)
    - DIPH (DIP with heat sink)
    - SIP (Single In-line Package)
    - SIPH (SIP with heat sink)
    - ZIP (Zigzag In-line Package)
    - ZIPH (ZIP with heat sink)
    - PGA (Pin Grid Array)

- **Skinny** - In this packaging, the space between the terminal rows is 7.62mm.
  - SKDIP (Skinny DIP)
- **Shrink** - Similar to the standard ones but the lead pitch is 1.778 mm. Smaller in size, they use high pin density packaging.
  - SDIP (Shrink DIP)
  - SDIPH (Shrink DIP with heat sink)
  - SSIP (Shrink SIP)
  - SZIP (Shrink ZIP)

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Lecture 5

Modern Packaging Solutions

By: SALAM AL-ABASSI

2021/2022

- The raw material for silicon manufacture is sand.
- The sand is heated in a furnace containing a source of carbon.

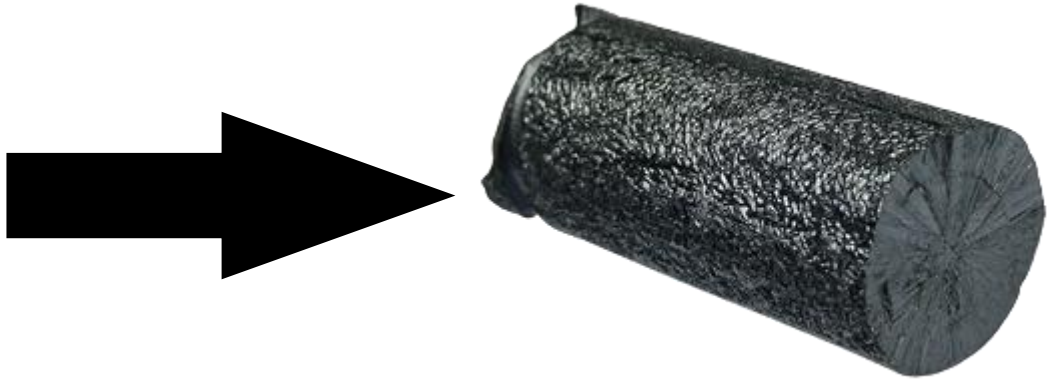
$$2C + SiO2 \longrightarrow (MGS)\ Si\ (98\%) + 2CO,$$

- Raw Material and Purification(EGS)

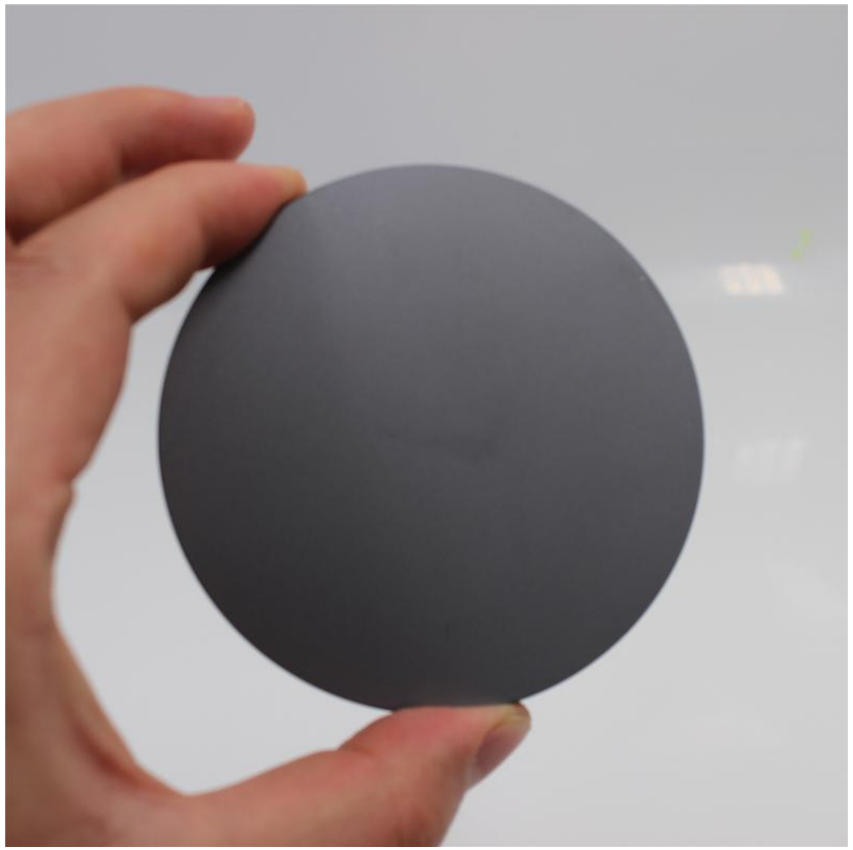
$$Si\ (s) + 3HCl\ (g) \longrightarrow SiHCl3\ (g) + H2\ (g) + heat$$

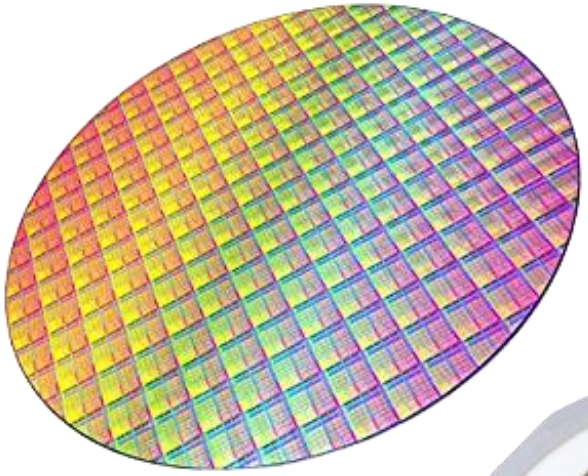
- To convert the SiHCl3 back into purified Si a CVD (Chemical Vapor Deposition) process is used (in a hydrogen atmosphere).

$$2SiHCl\ (gas) + 2H2\ (gas) \longrightarrow 2Si\ (solid) + 6HCl\ (gas)$$

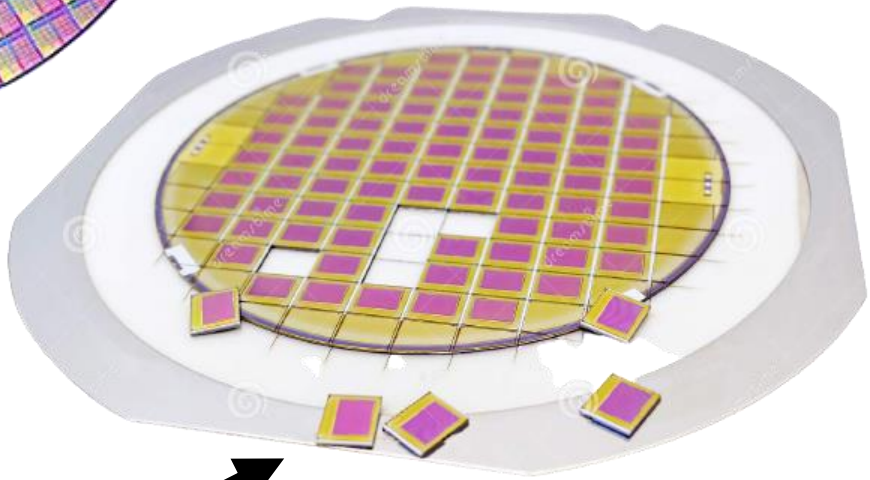


- **MONOCRYSTAL SILICON GROWTH**
- **Finally, Silicon Wafer is ready**



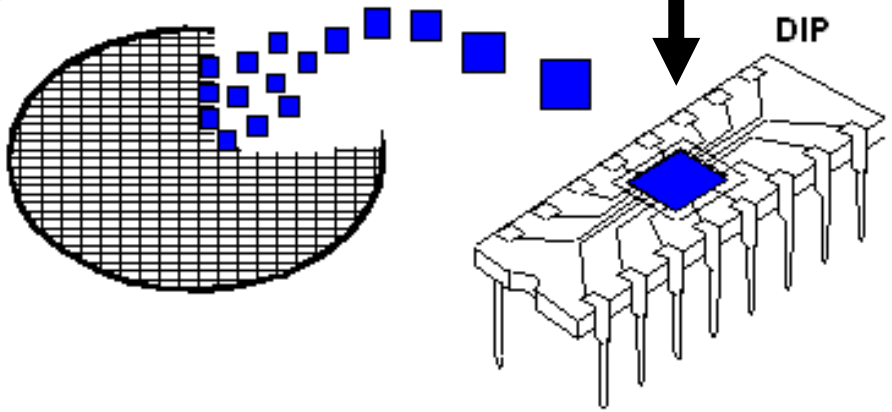


Silicon Wafer

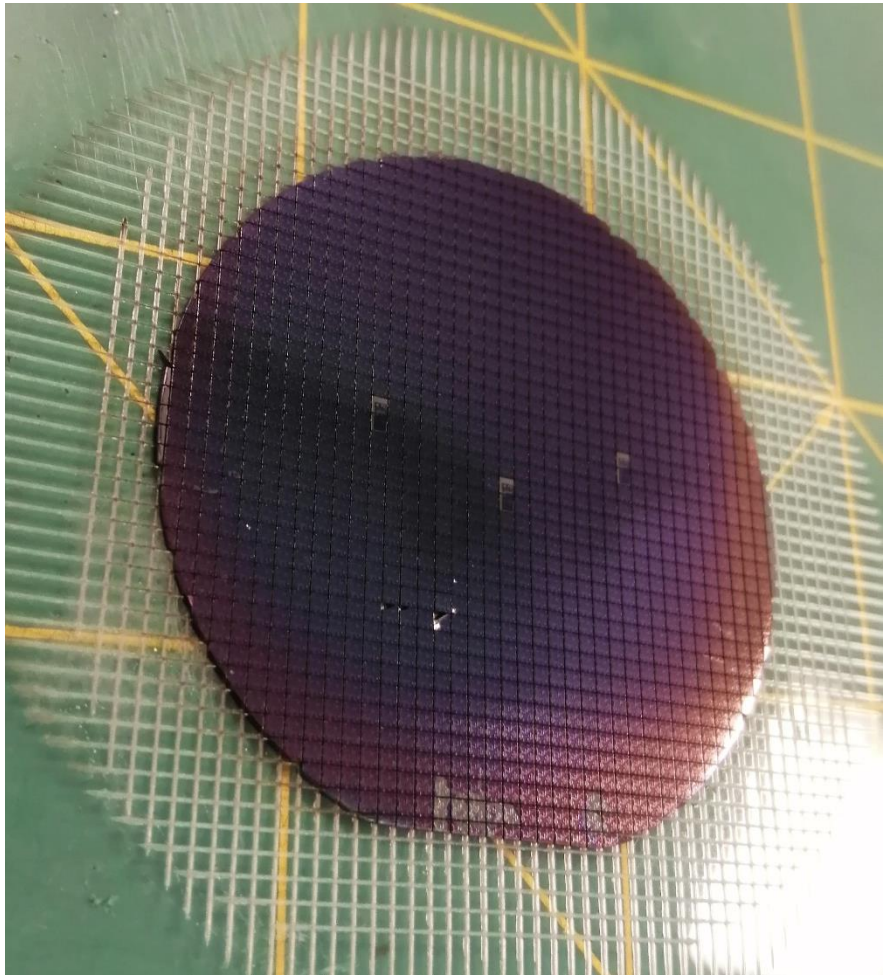


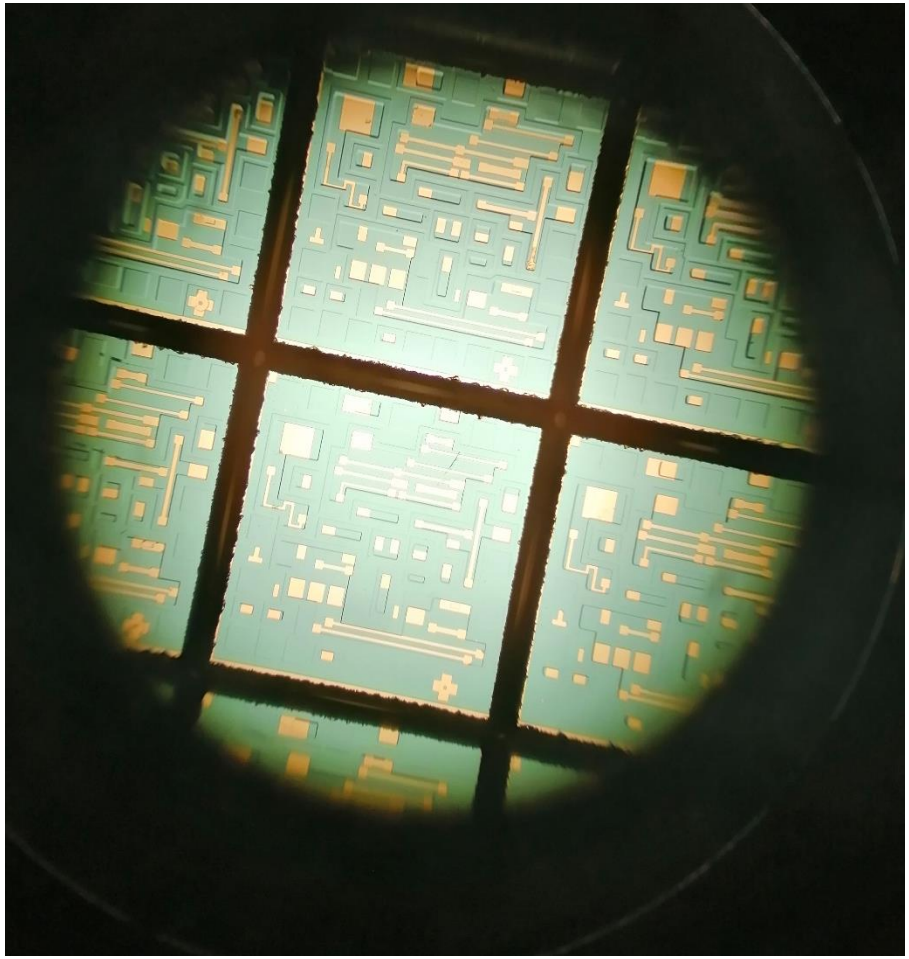
Die
(contains an integrated circuit)

Integrated Circuit
after packaging

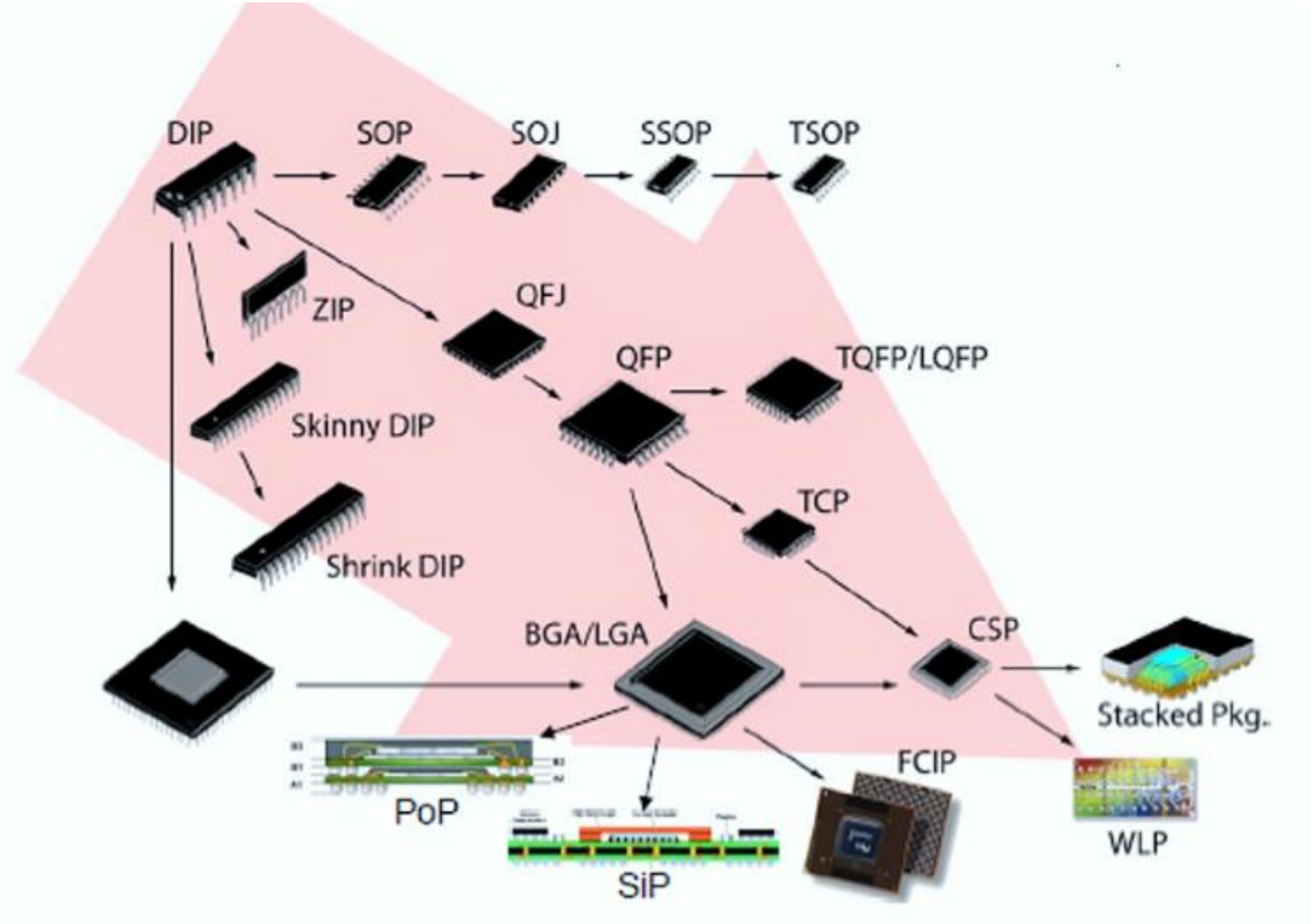


Example

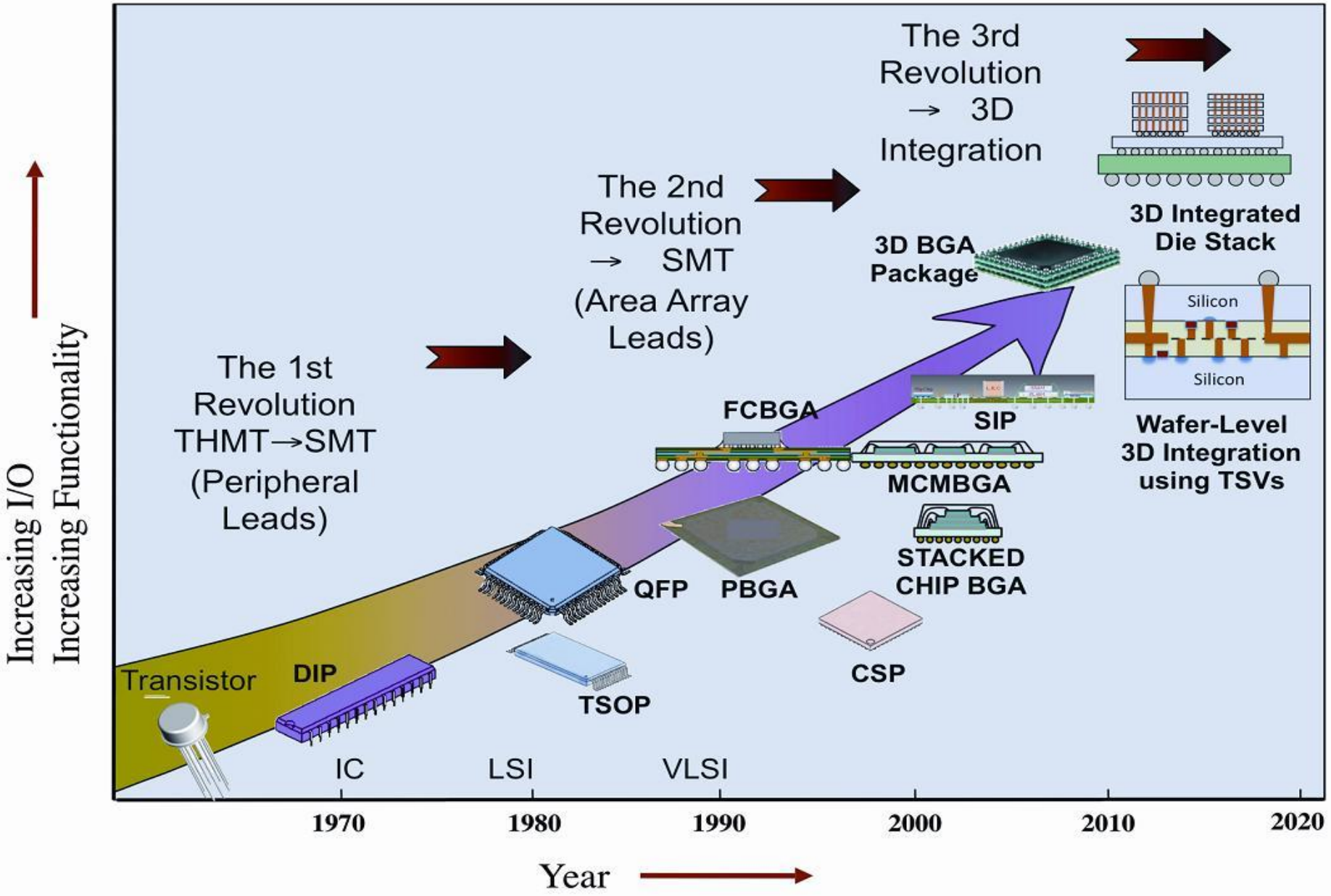




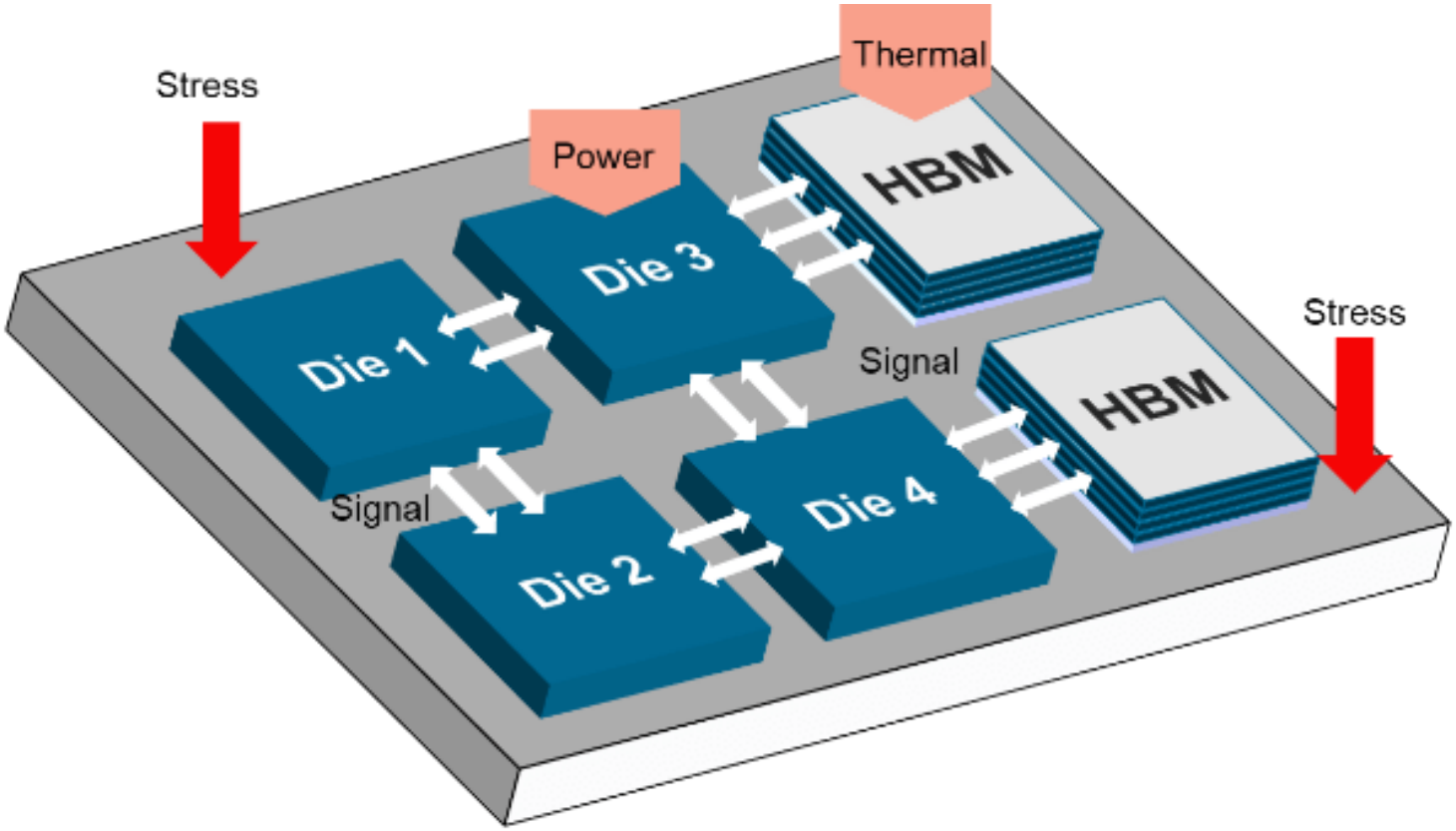
Packaging Technology Evolution



Packaging Technology Evolution

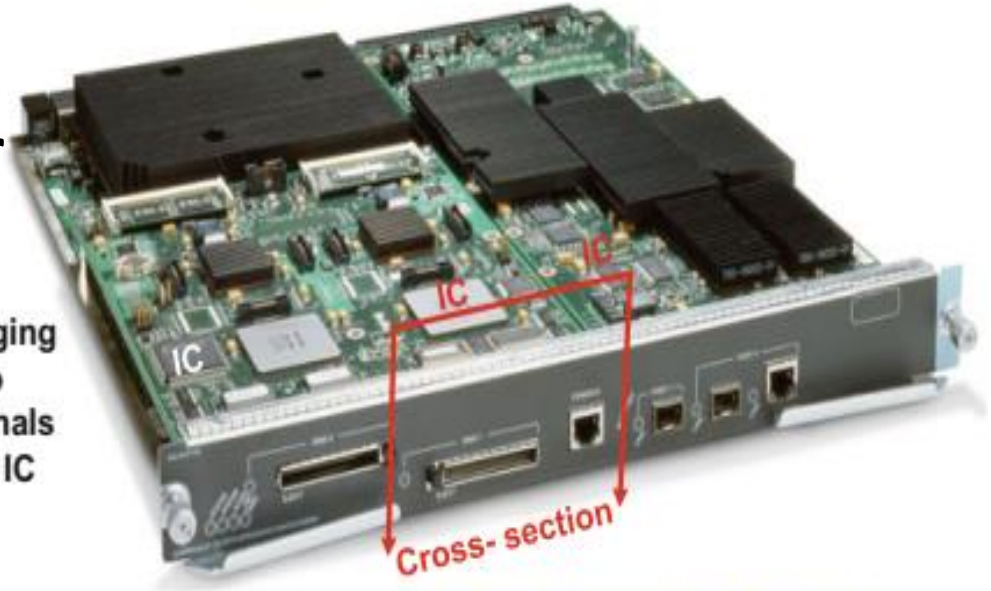


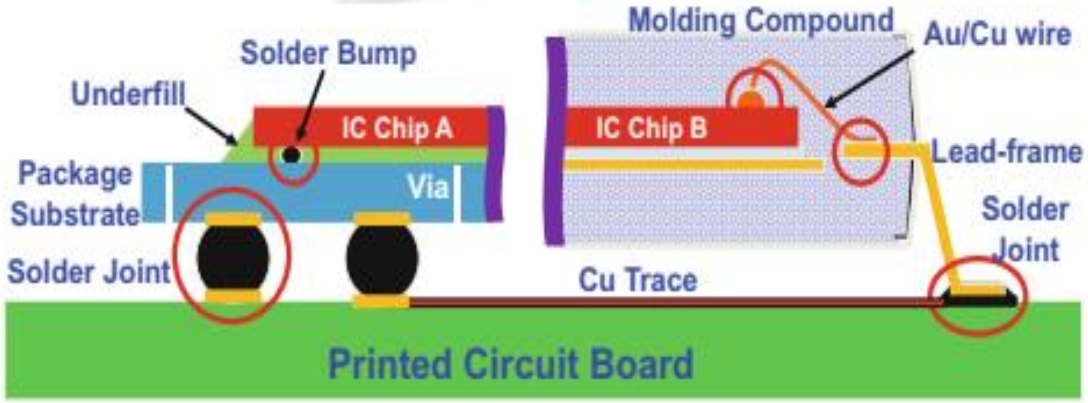
- **Identifying and accommodating the electrical, mechanical and thermal requirements inherent in the IC,**
- **Selecting those manufacturing technologies that incorporate attributes that will contribute to an end product that is “smaller, better, and cheaper”.**



- **Typical electronic product.**
- **It consists of printed circuit boards (PCBs) with some semiconductor integrated circuit (IC) chip components.**
- **IC chip is not an isolated island.**
- **It must communicate with other IC chips in a circuit through an input/output (I/O) system of interconnects.**

One of the packaging functions is to distribute the signals onto and off the IC chip.





Why Packaging?

- **The IC chip and its embedded circuitry are sensitive, requiring the package to both carry and protect it.**
- **the major functions of the semiconductor packaging are, for example :**

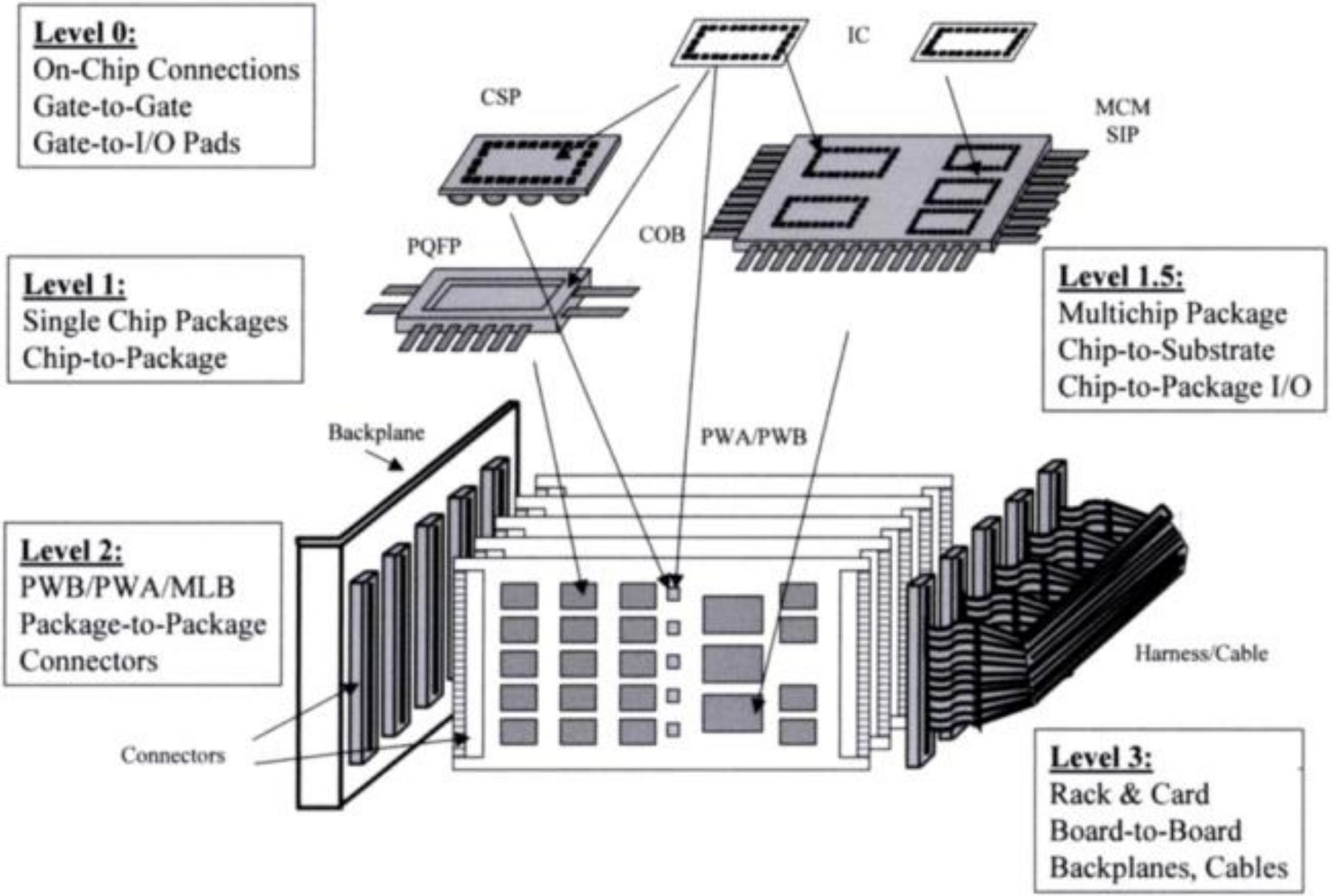
  (1) to provide a path for the electrical current that powers the circuits on the IC chip;

  (2) to distribute the signals onto and off the IC chip;

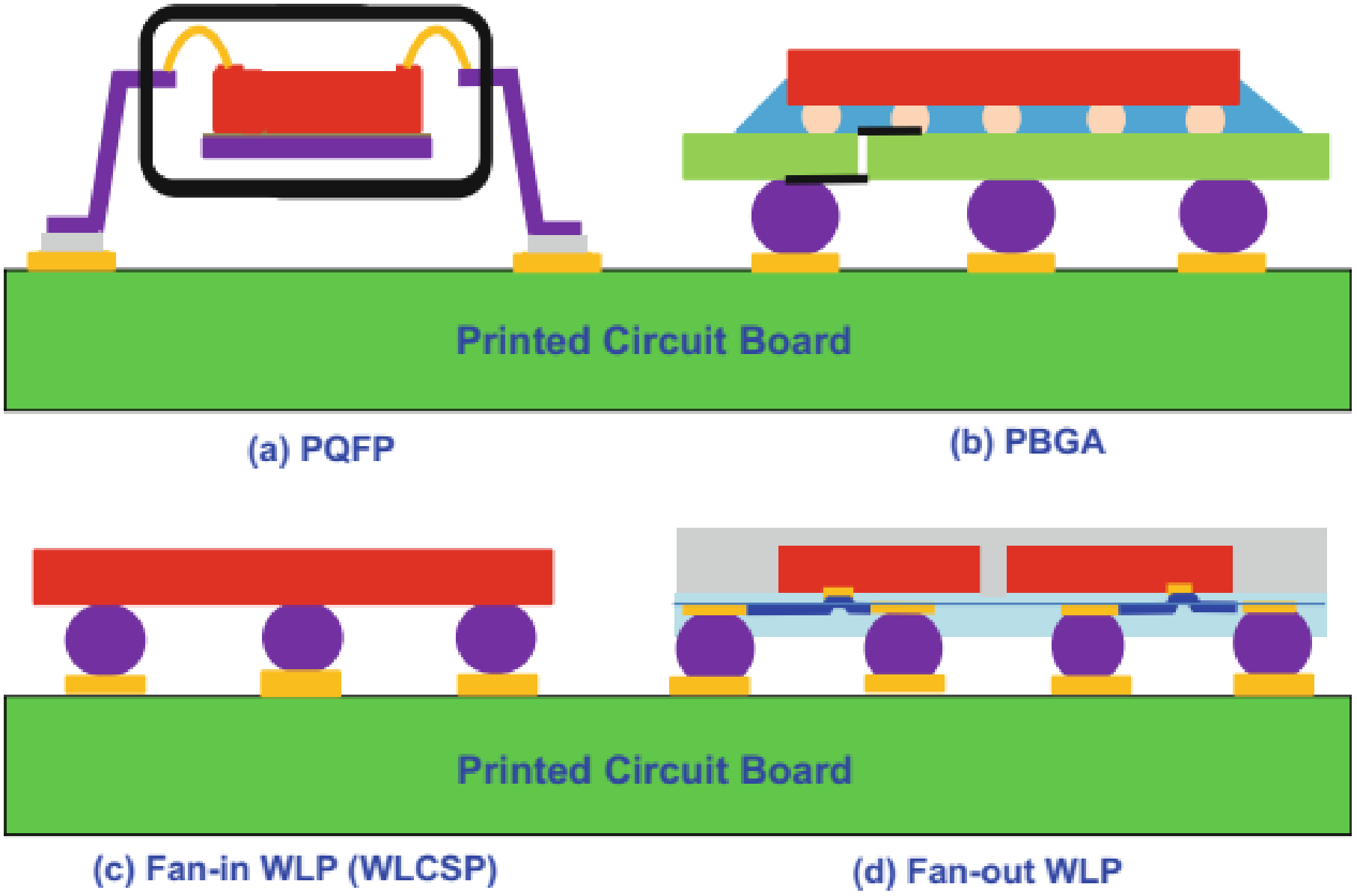
  (3) to remove the heat generated by the circuits on the IC chip;

  (4) to support and protect the IC chip from hostile environments.

Level of Semiconductor Packaging

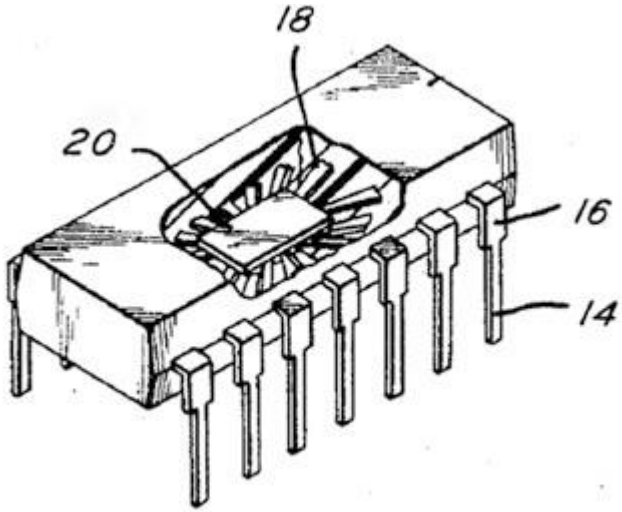


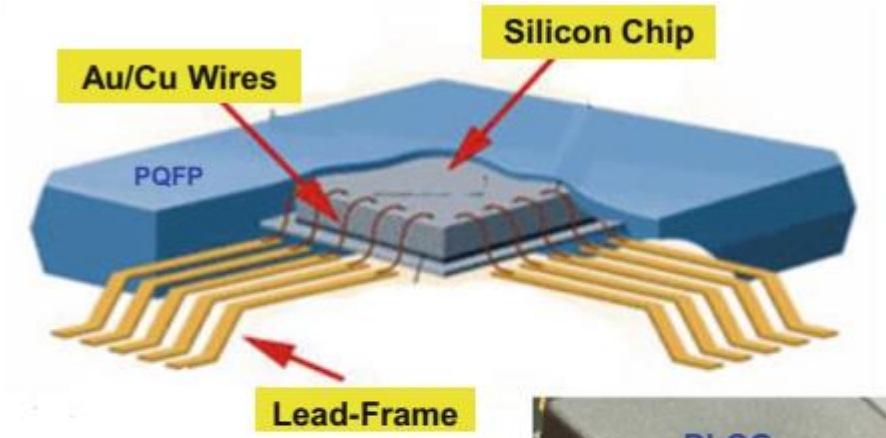
Different semiconductor packaging

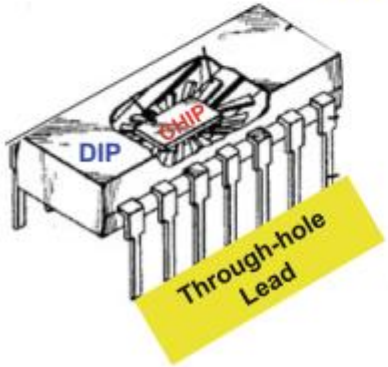


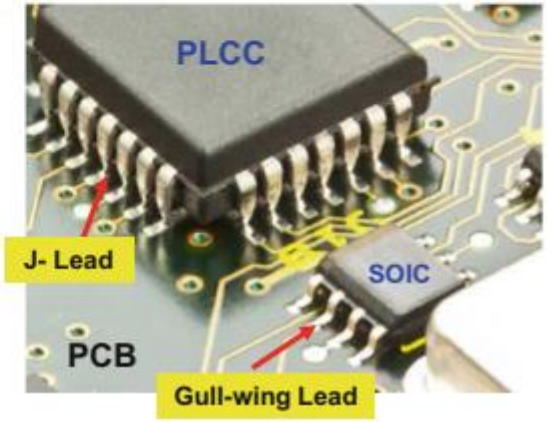
Leadframe

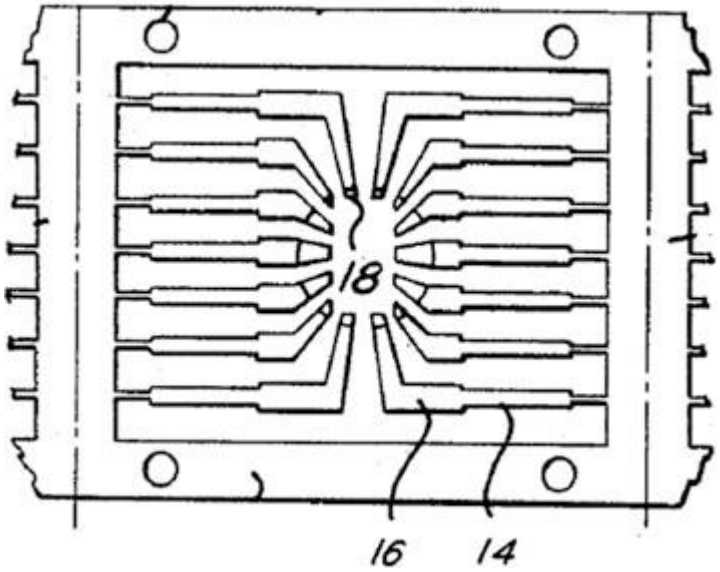
- July 17, 1967, by Kauffman.
- 14,16 are leadframes
- 18 is terminal ends of leadframes
- 20 is a chip





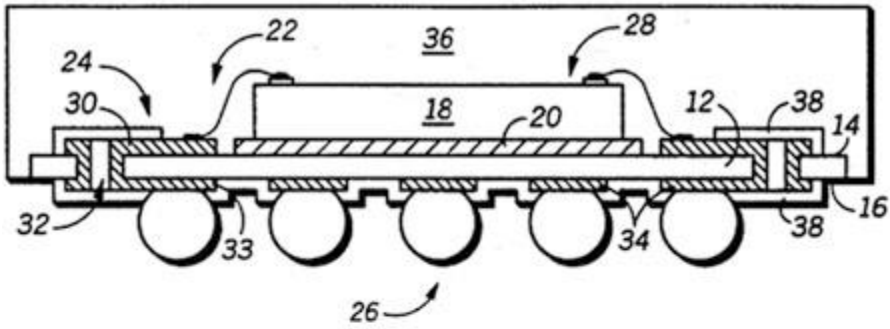




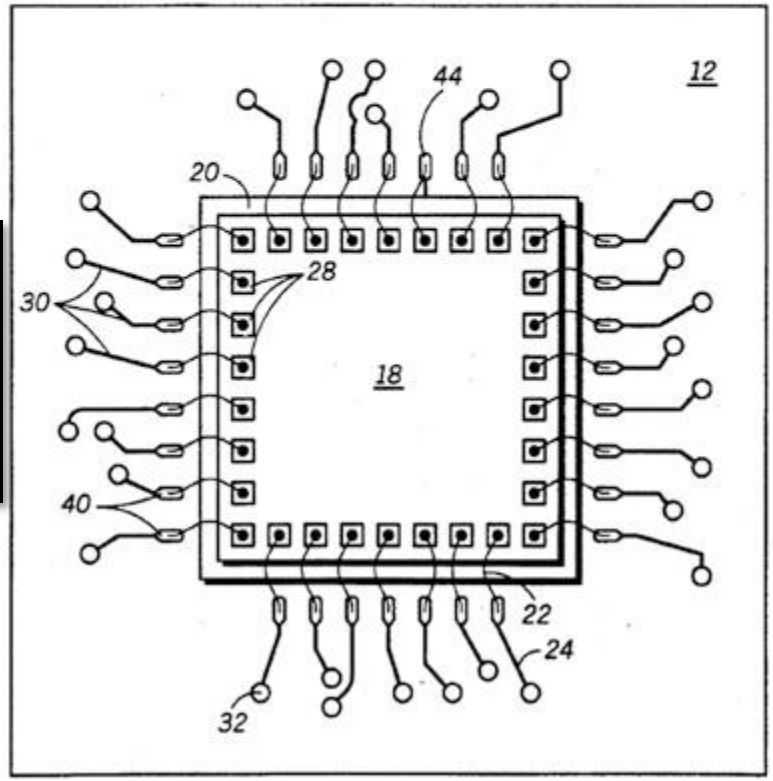


Organic Substrate with Solder Balls

- March 2, 1992, by Paul Lin, Mike McShane, and Howard Wilson
- 12 is a substrate (organic carrier).
- 26 is solder balls (area array).
- 18 is a chip
- 22 is wire bond
- 32 is used to connect the top layer with bottom layer



The over molded pad array carrier (OMPAC) package which is the first PBGA



The advantages of PBGA over leadframe are:

(1) less package area for the same package pin count and thus less PCB real estate,

(2) higher pin counts,

(3) lower profile,

(4) better in handling (no-bend leads),

(5) better coplanarity,

(6) better assembly yield because the forgiving of self-aligning characteristic of the surface tension of molten solder ball during reflow,

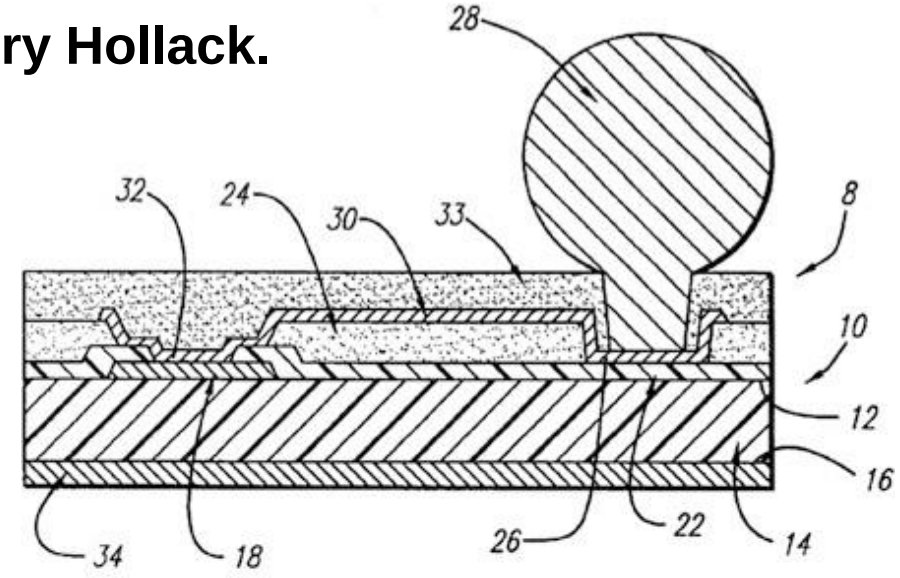
(7) better in rework,

(8) smaller inductance because of the short runs between the chip and the solder balls on the bottom of the substrate,

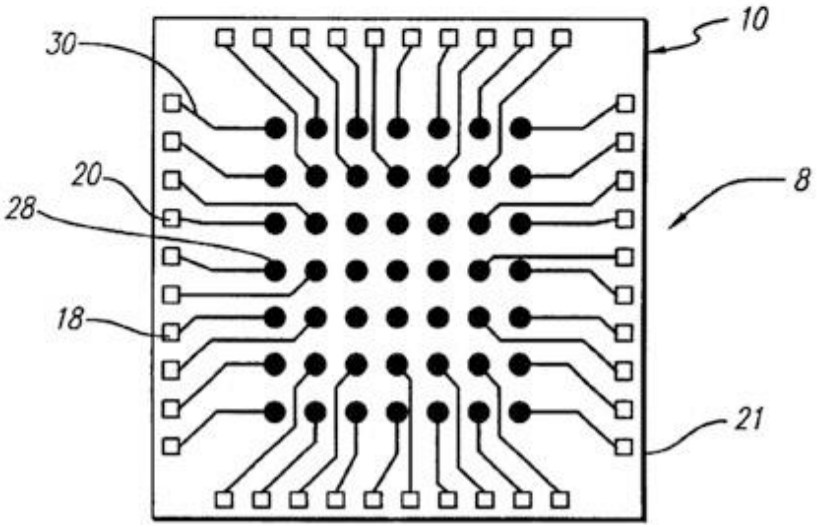
(9) smaller reflections and noise levels, respectively, by matching the trace length with the output impedance,

(10) better heat dissipation with copper power and ground planes

- July 13, 1998, Peter Elenius and Harry Hollack.
- 30 is redistribution layer (RDL).
- 18,20 are bond pads.
- 10 is a chip.
- 14 is a wafer
- 28 is solder balls
- 32 is the electrical contact



- Leadframe, substrate and underfill are eliminated



- The packages made by the fan-in WLP are called wafer-level chip scale package (WLCSP)

The advantages of WLCSPs over PBGA packages are

(1) lower cost,

(2) Lover profile,

(3) small form factor,

(4) simpler structure,

(5) lighter,

(6) less assembly steps,

(7) better electrical performance,

(8) eliminate the substrate, underfill, and one level of wafer bumping.

- **October 31, 2001, by Harry Hedler, Thorsten Meyer, and Barbara Vasquez**

34a-f are RDLs.

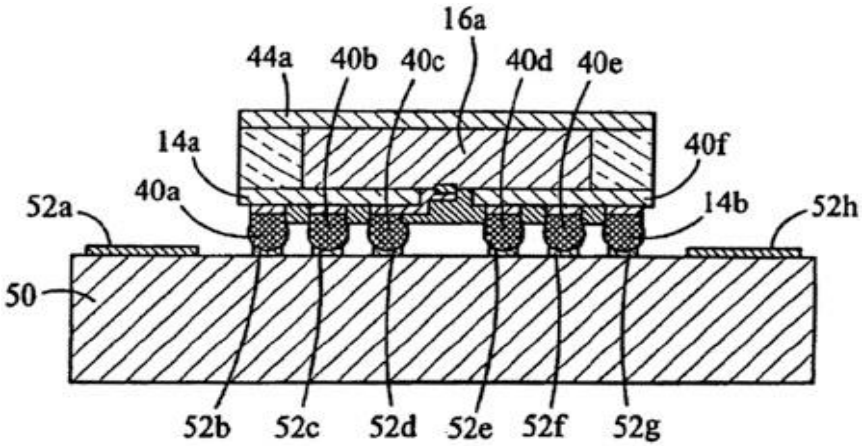
22s are metal pads.

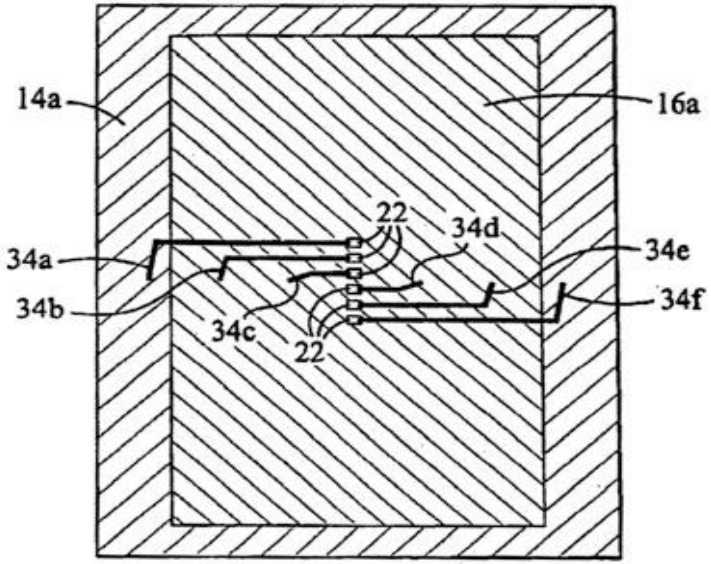
16a is a chip

40a-f are solder balls

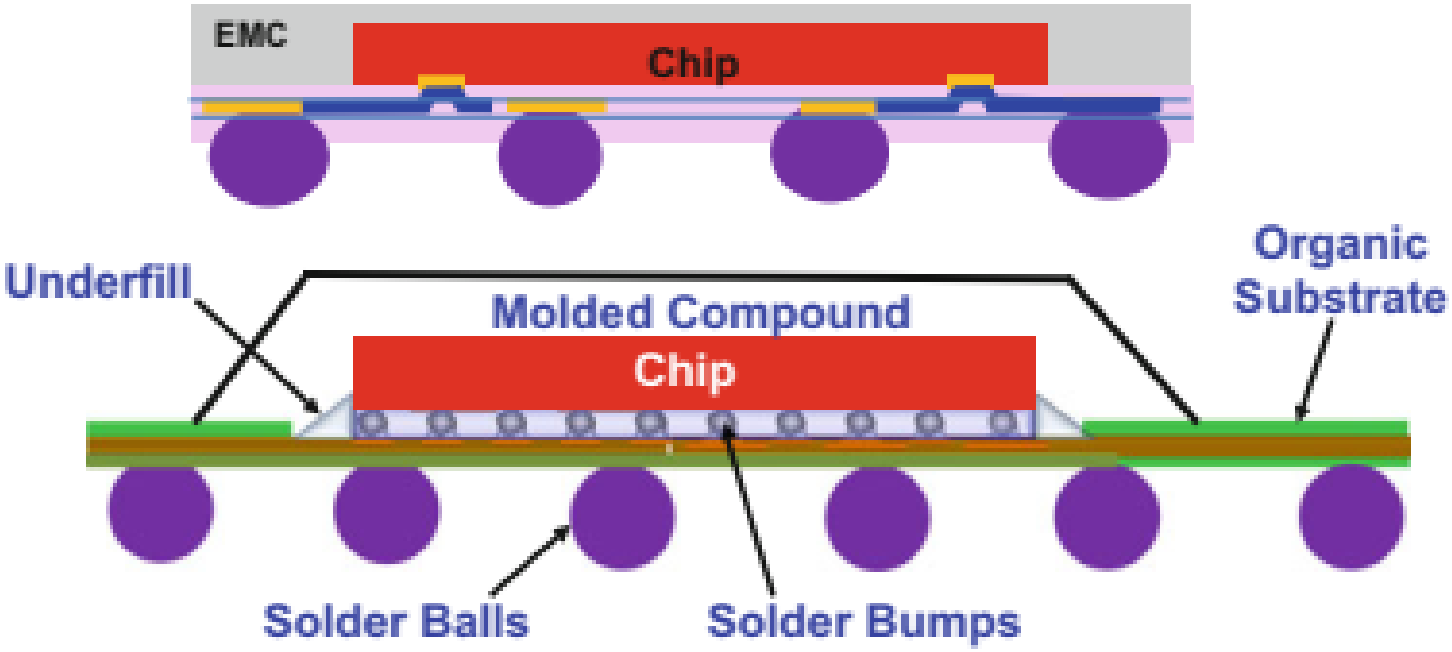
52b-g are metal pads.

14a-b are dielectric layers.



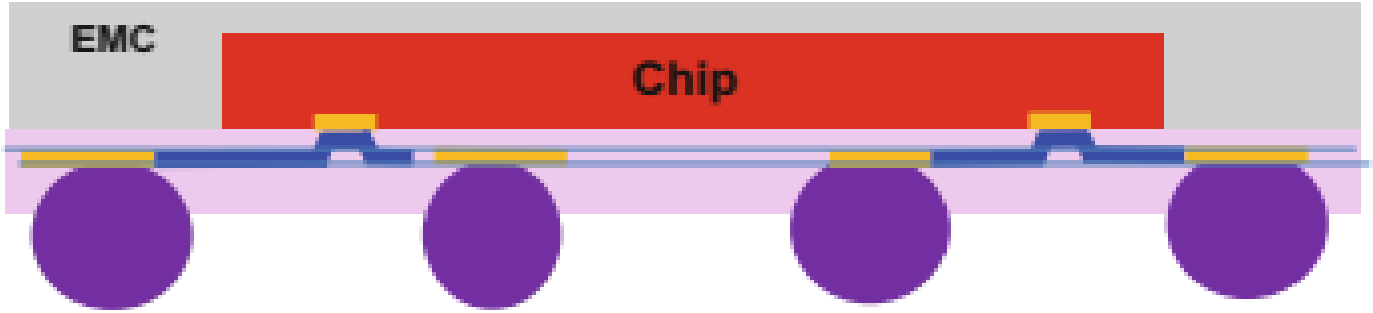


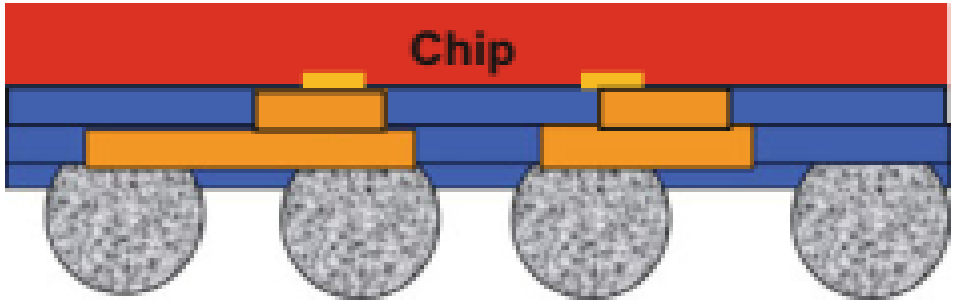
Advantages of fan-out WLP over fcPBGA



(1) lower cost
(2) lower profile
(3) eliminating the substrate
(4) eliminating the wafer bumping
(5) eliminating the flip chip reflow
(6) eliminating the flux cleaning
(7) eliminating the underfill
(8) better electrical performance
(9) better thermal performance
(10) easier to go for system-in-package (SiP) and 3D IC packaging

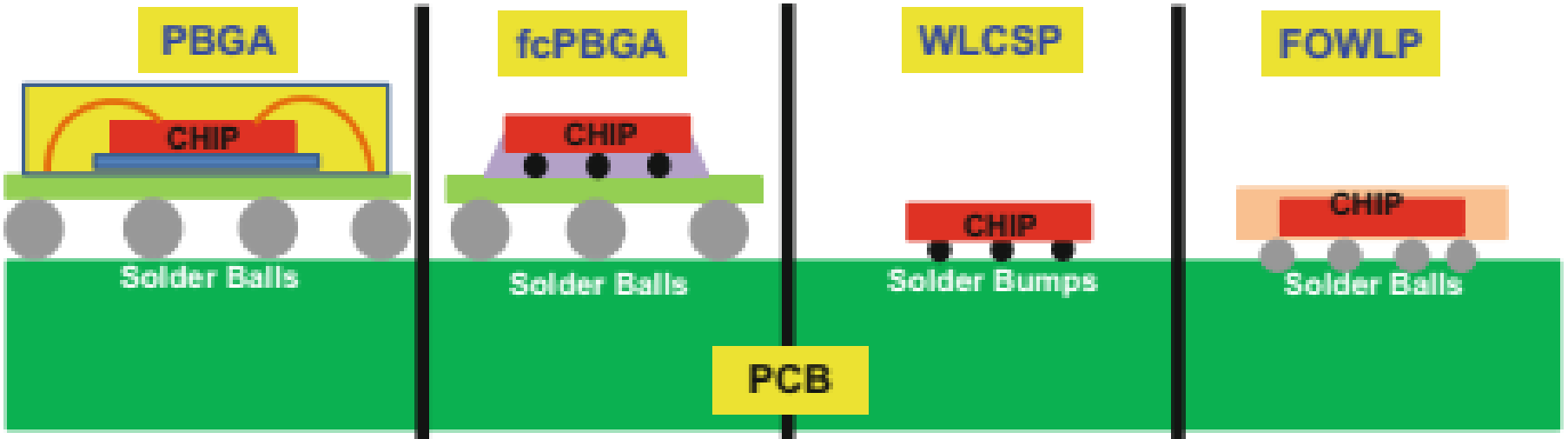
Advantages of fan-out WLP over fan-in WLP





(1) the use of known good die (KGD)
(2) better wafer-level yield
(3) using the best of silicon
(4) multichip
(5) embedded integrated passive devices
(6) more than one RDL
(7) higher pin counts (or die shrink)
(8) better thermal performance
(9) easier to go for SiP and 3D IC packaging
(10) higher PCB level reliability.

Ball/Bump Pitch/Size of PBGA, fcPBGA, WLCSP, and FOWLP



Solder Ball Pitch:
1.27, 1, 0.8, and 0.65mm

Solder Ball Pitch:
1.27, 1, 0.8, 0.65, 0.5, and 0.4mm

Solder Bump Pitch:
0.5, 0.4, 0.35, and 0.3mm

Min. Bump Size:
0.15mm for 0.3mm-pitch

Solder Ball Pitch:
0.5, 0.4, 0.35, and 0.3mm

Min. Ball Size:
0.17mm for 0.3mm-pitch
.225mm for 0.35mm-pitch
0.25mm for 0.4mm-pitch
0.3mm for 0.5mm-pitch

References

- Fan-Out Wafer-Level Packaging (John H. Lau)
- Integrated Circuit Packaging, Assembly and Interconnections (William J. Greig)

Budapest University of Technology and Economic
Department of Electron Devices

Circuit Environment

Lecture 6

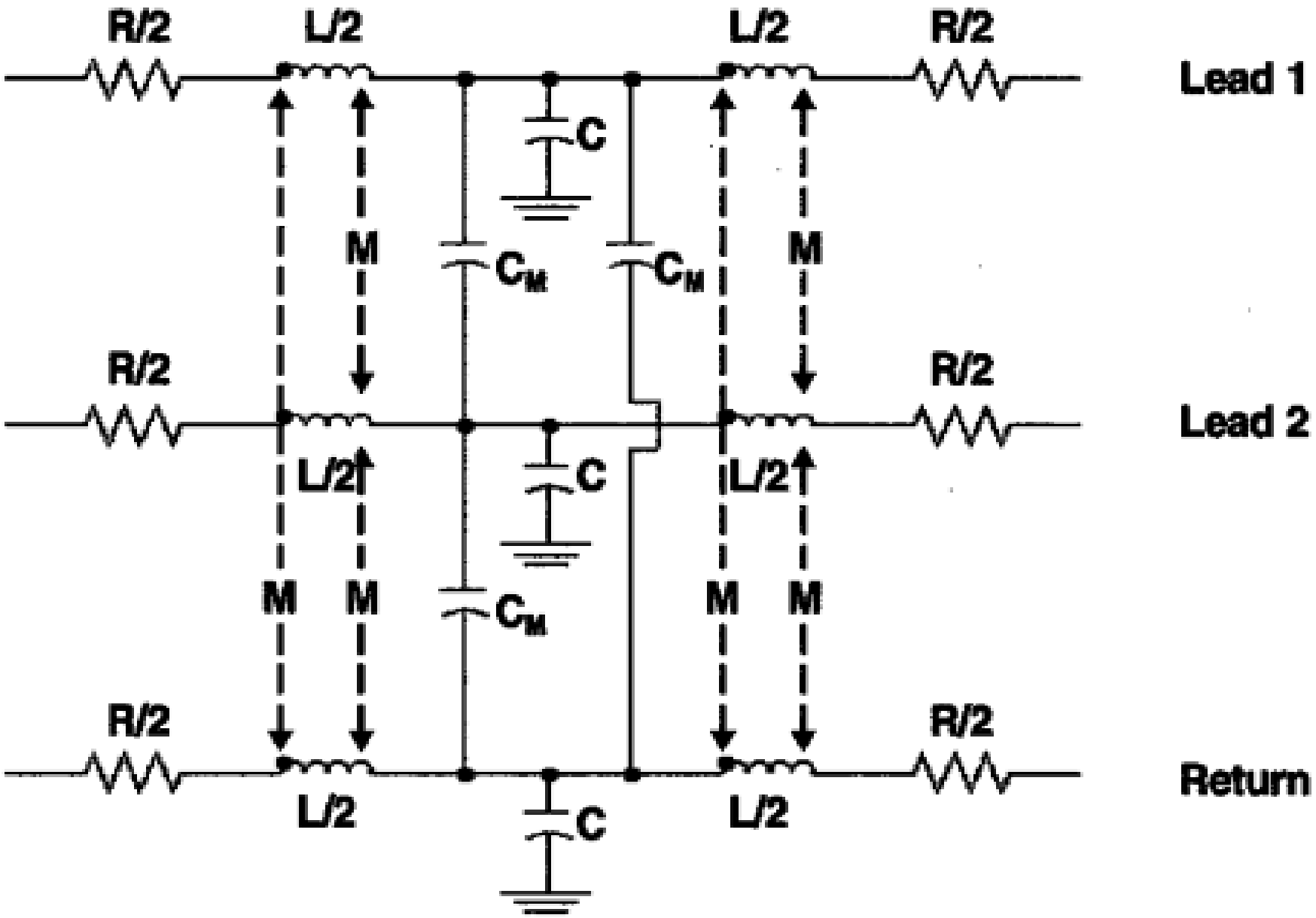
Parasitic effects of packaging

By: SALAM AL-ABASSI

2021/2022

Packaging Parasitic

- **The effects of packaging on RFICs.**
- The effects of packaging on thermal management of ICs


R/2
L/2
L/2
R/2
Lead 1
C
M
C_M
C_M
M
R/2
R/2
Lead 2
L/2
C
L/2
M
M
C_M
M
M
R/2
R/2
Return
L/2
C
L/2

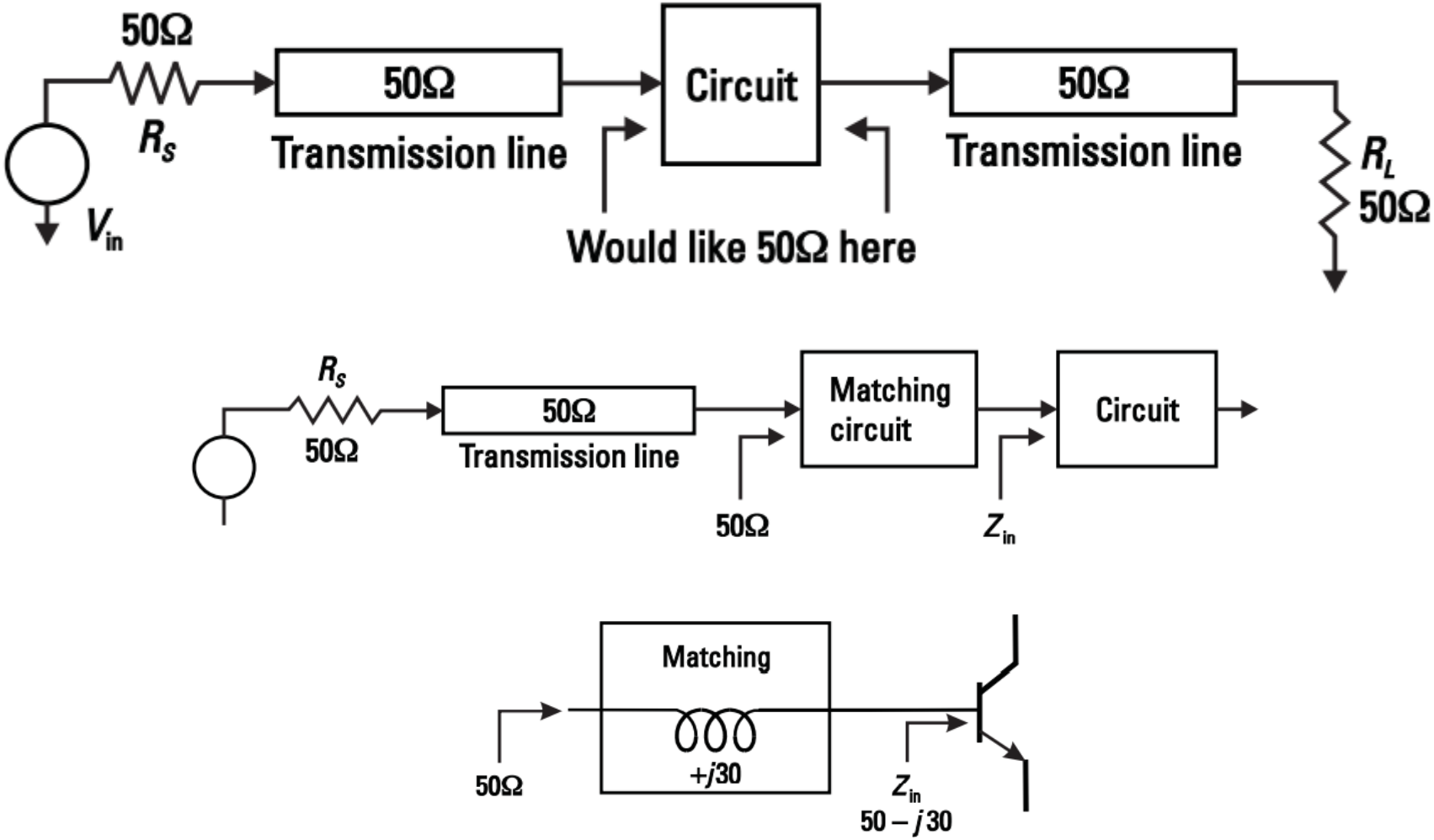
Radio frequency integrated circuits (RFIC): are the devices that work at range of frequencies from 20kHz to 300GHz.

- **in order to design radio frequency (RF) communications integrated circuits (IC) in the gigahertz range, it must deal with:**
  1- **Transmission lines at chip interfaces.**
  2- **Impedance matching is addressed.**

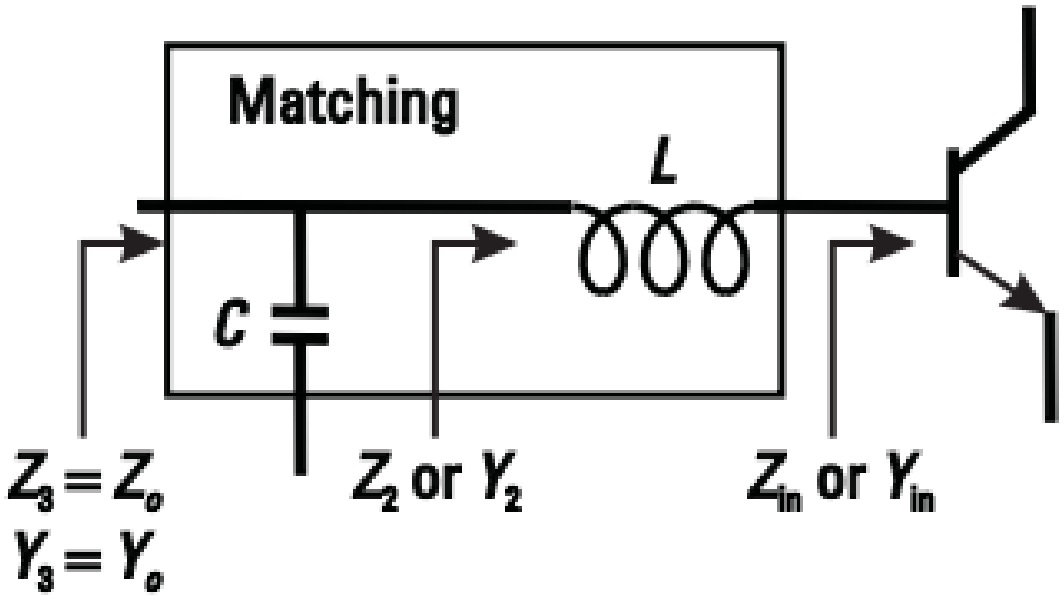
$$u_p = f\lambda \qquad \text{(m/s)}.$$

▶ When l/λ is very small, transmission-line effects may be ignored, but when $l/\lambda \gtrsim 0.01$, it may be necessary to account not only for the phase shift due to the time delay, but also for the presence of ***reflected*** signals that may have been bounced back by the load toward the generator. ◀

Impedance matching

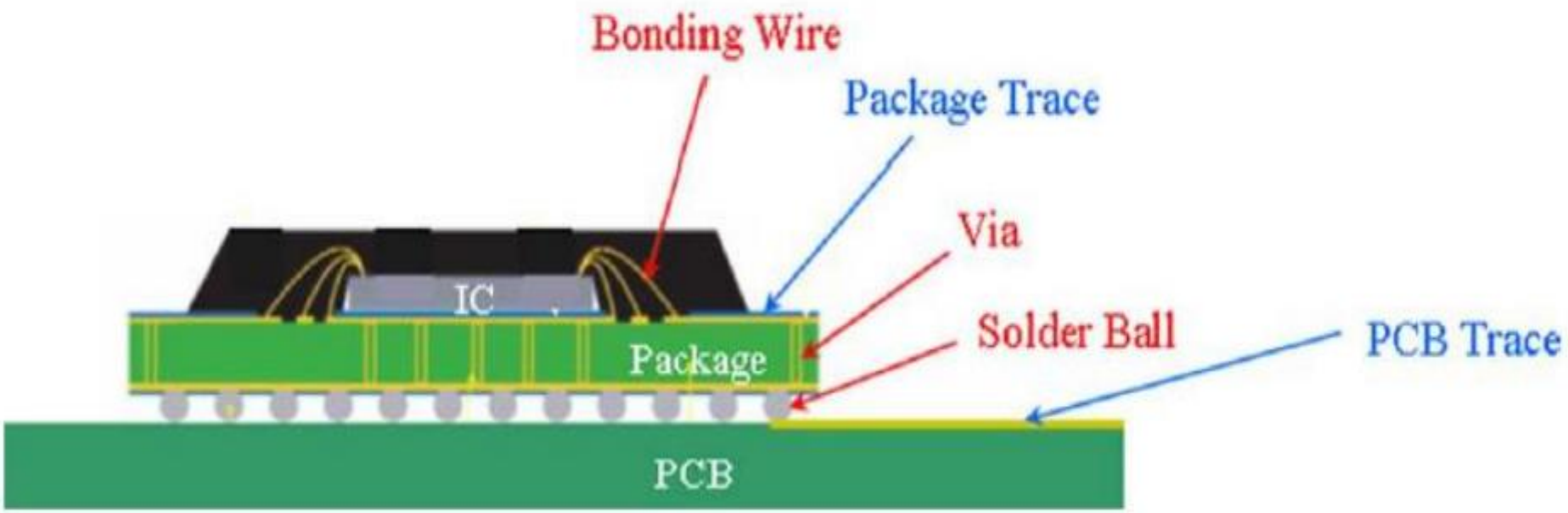


Use the matching network to match the transistor input impedance Zin = 40 – j30 Ω to Zo = 50Ω. Perform the matching at 2 GHz.



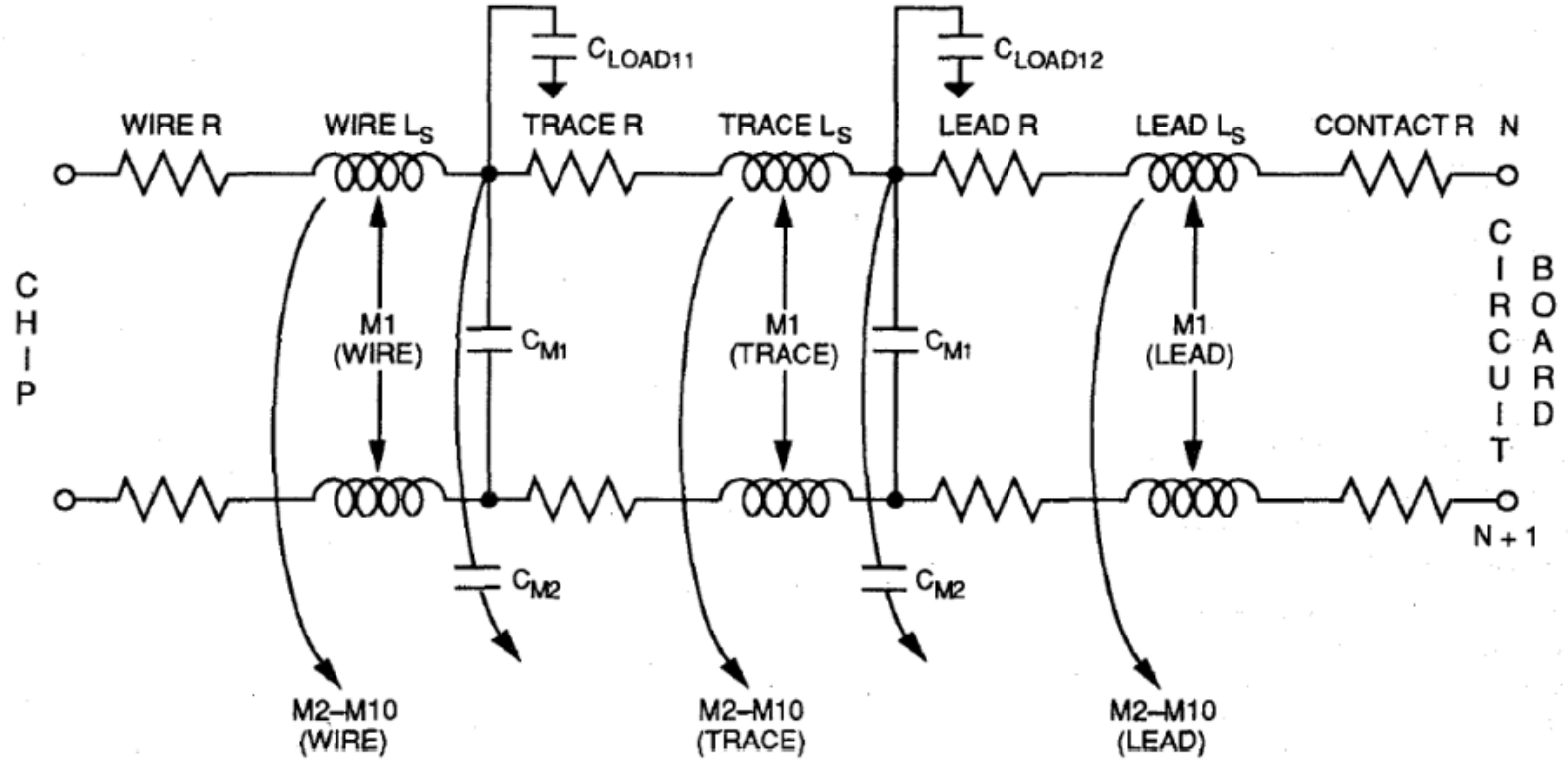
Bringing it all Together:

- When combining the packaged IC and the PCB, there are several parasitic factors the IC designer and the PCB designer must consider for a high-performance circuit.



Quad flat pack Equivalent electrical circuits

- Note that there are a number of interacting mutual inductances (M), mutual capacitances (CM), as well as self inductances (Ls), self capacitances(C) and resistances (R).



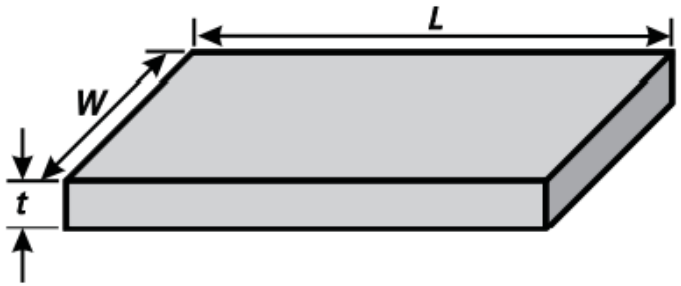
Quad flat pack (QFP) package

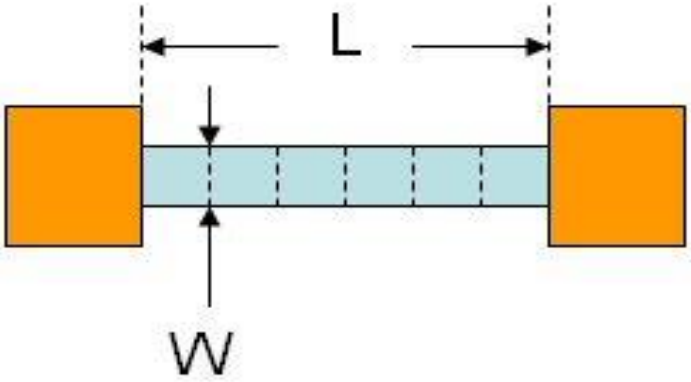
(self inductance, L; mutual inductance, Lm; self capacitance, C; mutual capacitance, Cm; input output pad capacitance, Cio; and resistance, R)

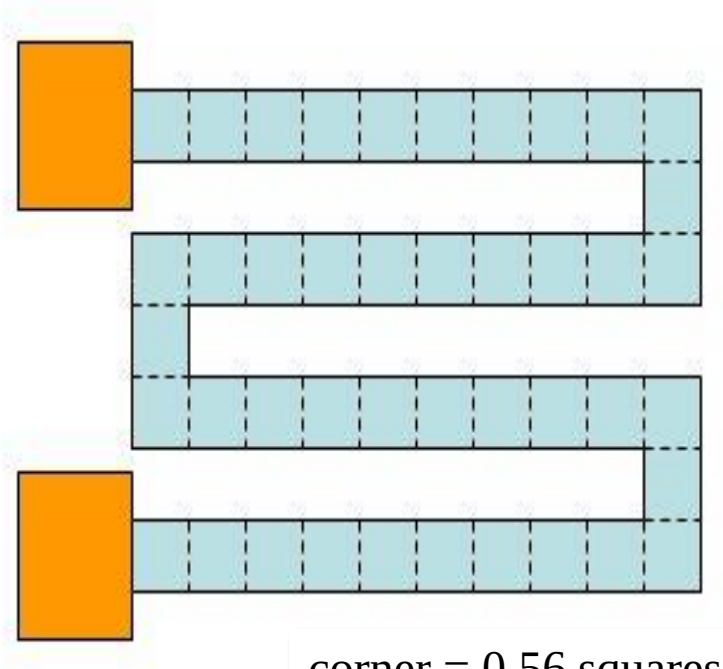
- Self inductance: is the inductance of the wire itself.
- Mutual inductance: is the inductance between adjacent wires.
- Self capacitance: is the capacitance between the wire and ground plane.
- Mutual capacitance: is the capacitance between two wires.
- Cio: is the capacitance created by the IO pads of the die and its carrier where the bond wires are connected.
- Resistance: is simply the resistance of the wire which is affected by the skin depth of the wire.
- Skin depth: is the depth that current is carried in wires which becomes shallower as frequency increases.

- Sheet resistance: (also known as surface resistance or surface resistivity) is a common electrical property used to characterize thin films of conducting and semiconducting materials.

$$\rho = \frac{1}{\sigma} \qquad R = \frac{\rho L}{Wt} \qquad \rho_s = \frac{\rho}{t} = R\left(\frac{W}{L}\right)$$







corner = 0.56 squares

- Skin effect is usually described as the tendency of current to flow on the surface (skin) of a conductor as frequency increases.
- Because the inner regions of the conductor are less effective at carrying current than at low frequencies.
- The useful cross-sectional area of a conductor is reduced, thereby producing a corresponding increase in resistance.

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}}$$

Skin depth of some common metals over the frequency band of interest.

Skin Depth of Various Metals at Various Frequencies

Metal	ρ ($\mu\Omega \cdot$ cm)	500 MHz	1 GHz	2 GHz	5 GHz	10 GHz
Gold	2.44	3.5 μm	2.5 μm	1.8 μm	1.1 μm	0.79 μm
Tungston	5.49	5.3 μm	3.7 μm	2.6 μm	1.7 μm	1.2 μm
Aluminum	2.62	3.6 μm	2.6 μm	1.8 μm	1.2 μm	0.82 μm
Copper	1.72	3.0μm	2.1μm	1.5μm	0.93μm	0.66μm
Silver	1.62	2.9 μm	2.0 μm	1.4 μm	0.91 μm	0.64 μm
Nickel	6.90	5.9 μm	4.2 μm	3.0 μm	1.9 μm	1.3 μm

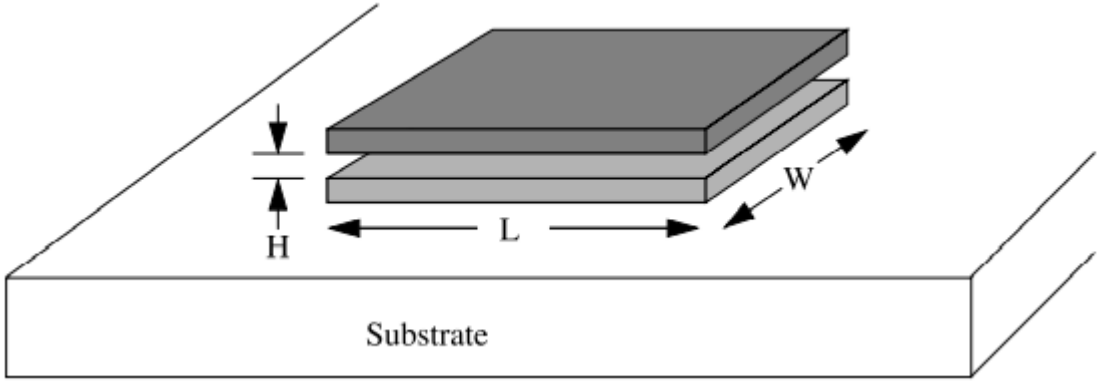
Example:

- A rectangular aluminum line has a width of 20 µm, a thickness of 3 µm, and a length of 100 µm. Compute the resistance of the line at dc and at 5 GHz assuming that all the current flows in an area one skin depth from the surface. Assume that aluminum has a resistivity of 3 µΩ.cm.

Ans:

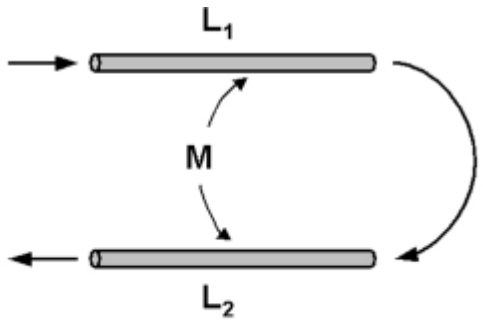
- All of the interconnect layers may be used to make traditional parallel plate capacitors

$$C \approx \varepsilon \frac{A}{H} = \varepsilon \frac{W \cdot L}{H},$$



- Dielectric layer tends to be rather thick (order of 0.5–1 µm), precisely to reduce the capacitance between layers

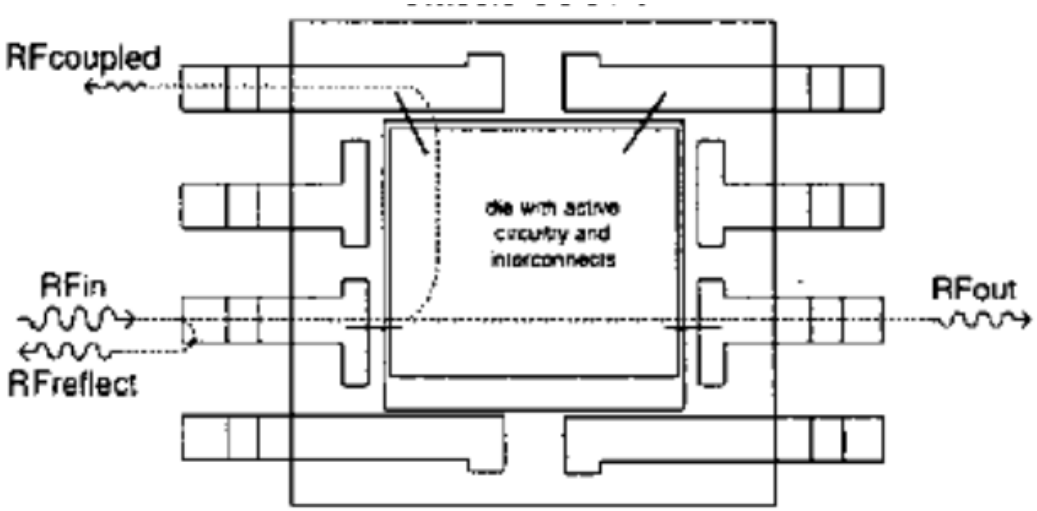
- Inductance (L) is defined as the relationship between the following for a closed current path:
  - flux linkage (Φ) and current flow (i): $\Phi = L \times i$
  - time varying voltage (v) and current (i): $v = L \times di/dt$
- On an IC package, signals propagate in and out through the signal leads and return through the power leads.
- The closed current path (or loop) is formed by signal leads together with power or ground leads.



$L_{LOOP} = L_1 + L_2 - 2M$

Parasitic Inductance

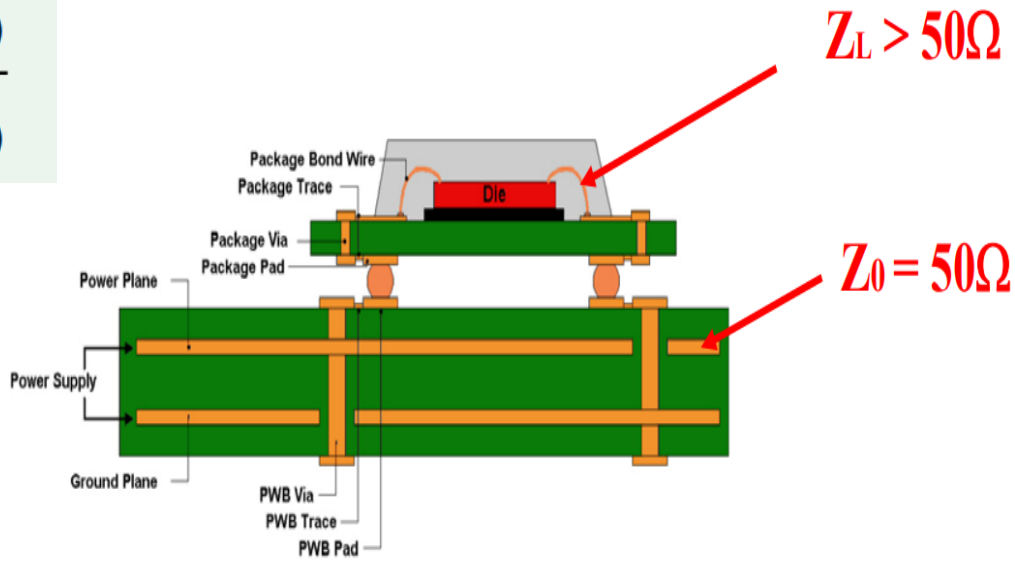
- Due to the non idealities (i.e.parasitic R, L, C) of packages.
- The RF input signal is reflected, transmitted and coupled throughout the die.
- Performance of ICs will be degradation in the form of:
  - -insufficient Return Loss(RL)
  - -excessive Insertion Loss(IL)
  - -reduced pin to pin isolation
  - -reduction of bandwidth
  - -linearity.



Why is packaging limiting performance?

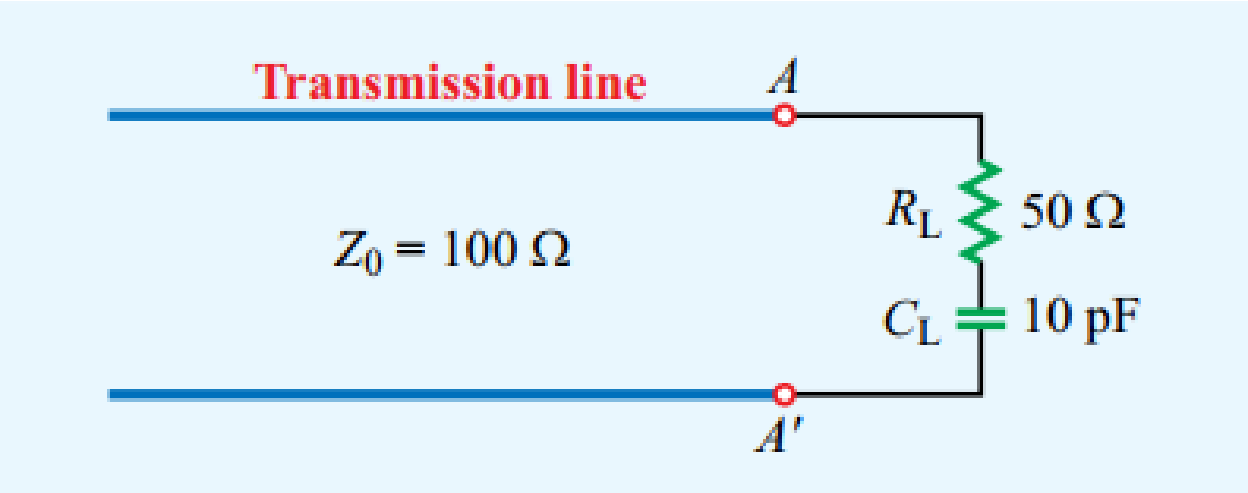
- Inductive Interconnect Leads to Reflections
  - Interconnect is not matched to system.
  - Reflections occur due to interconnect.

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0}$$



Example:

A 100Ω transmission line is connected to a load consisting of a 50Ω resistor in series with a 10pF capacitor. Find the reflection coefficient at the load for a 100 MHz signal.



Current Solution to Reflections

- Live with the Signal Path Reflections.

1) Run the signals slow enough so that reflections are small.

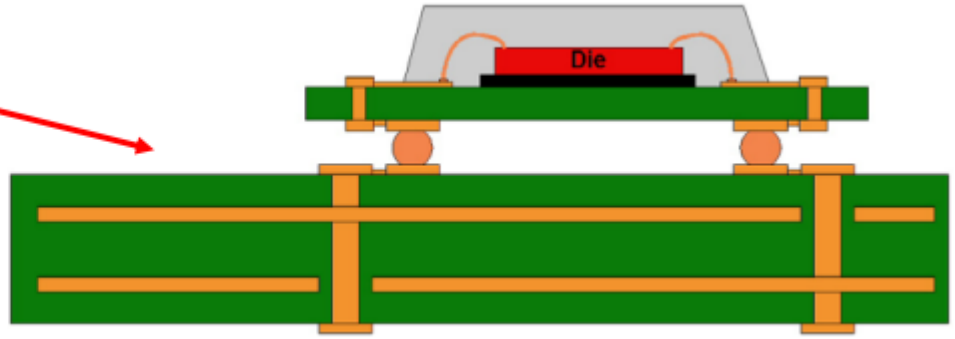
* Limits System Performance

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \quad < 10\%$$

2) Terminate Signals on the Mother board so that reflections are absorbed.

*This only eliminates primary reflections, the second still exists

On Mother Board Termination



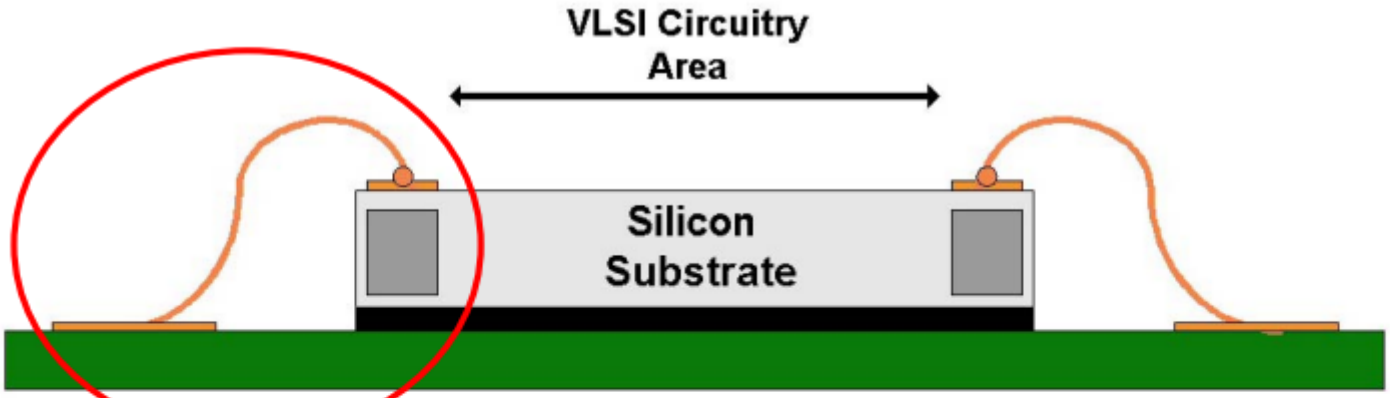
Add Capacitance Near Bond Wire to Reduce Impedance

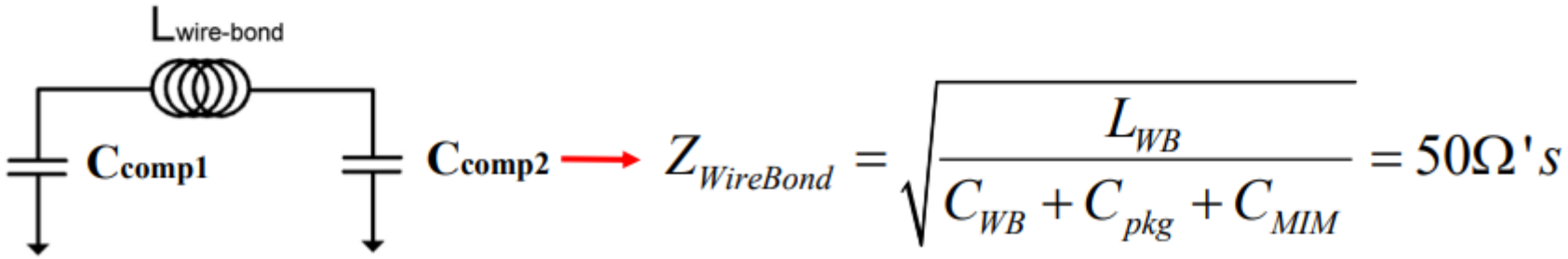
- Adding additional capacitance lowers the wire bond impedance
- Impedance can be matched to system, reducing reflections

$$Z_{WireBond} = \sqrt{\frac{L_{WireBond}}{C_{WireBond}}}$$

← Add Capacitance to lower Z

- Capacitance on the IC or Package is close enough to alter impedance

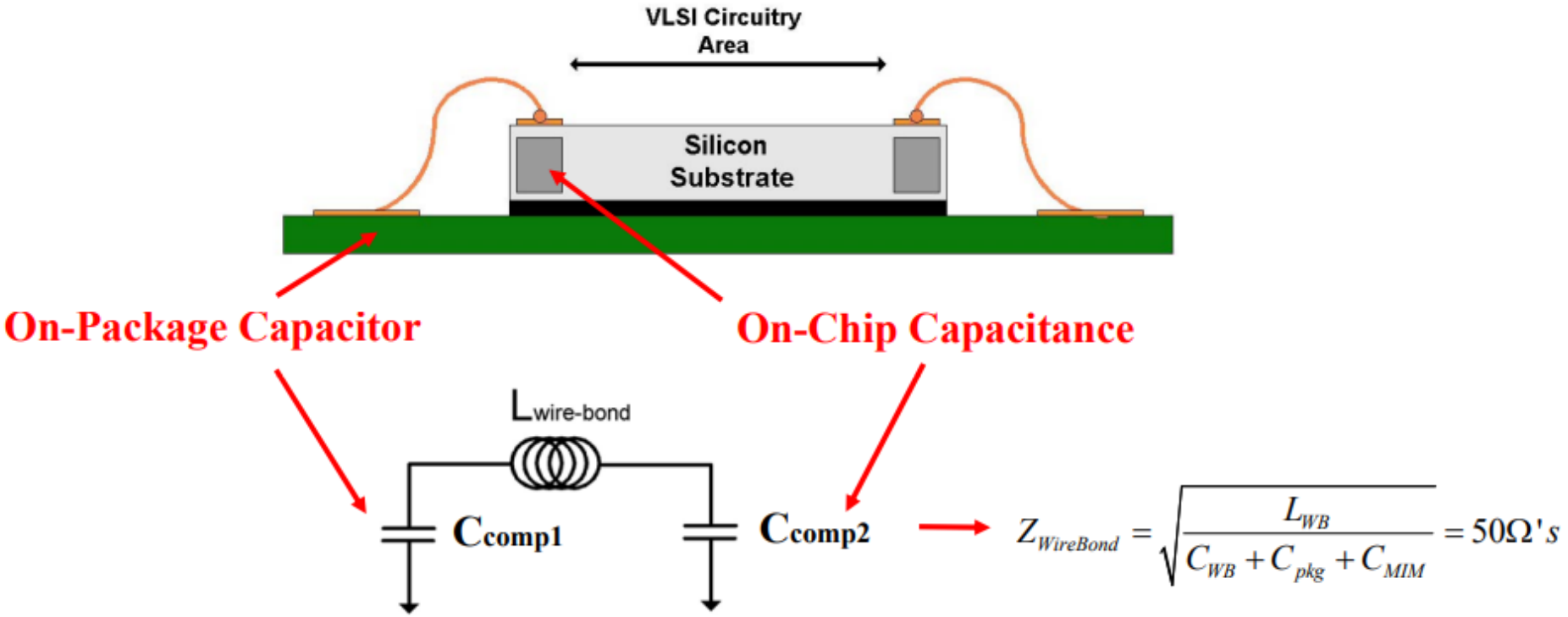




$$Z_{WireBond} = \sqrt{\frac{L_{WB}}{C_{WB} + C_{pkg} + C_{MIM}}} = 50\Omega's$$

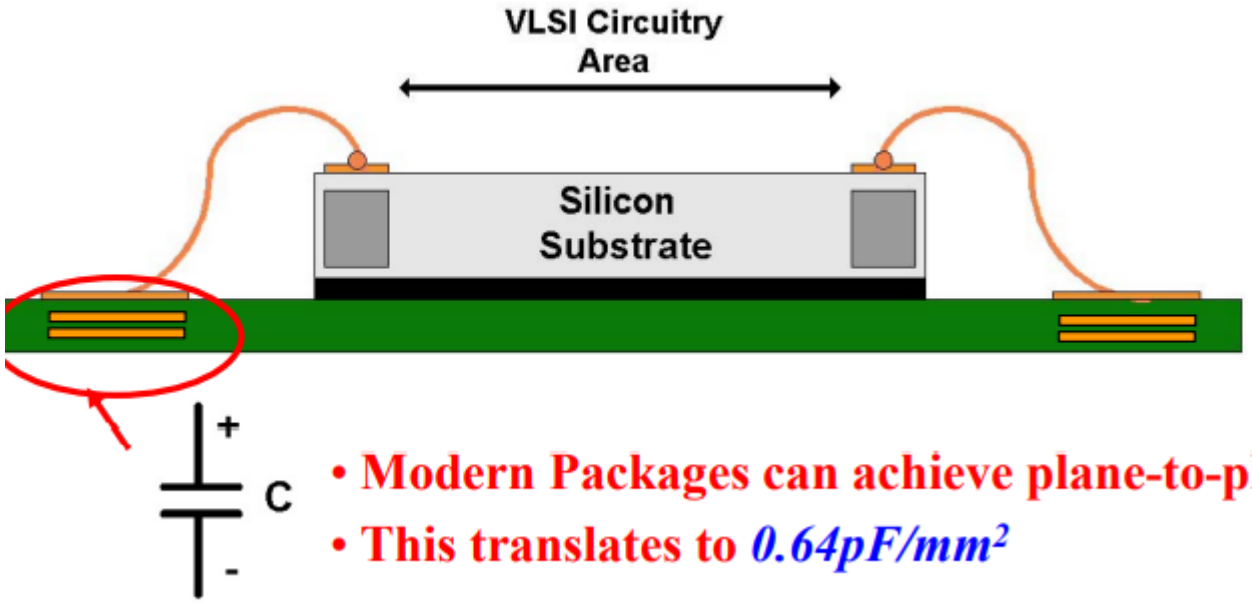
Capacitor values chosen prior to fabrication

- Equal amounts of capacitance are used on-chip and on-package.



On-Package Capacitors

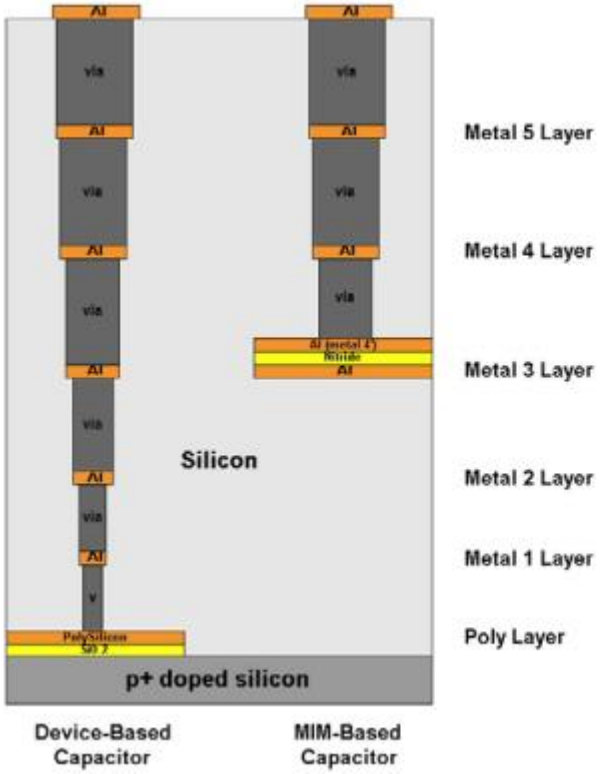
- Embedded capacitor construction is used
- No components are needed, reducing package cost
- Capacitance values needed can be implemented using this construction



- **Modern Packages can achieve plane-to-plane separations of *t=0.002”***
- **This translates to *0.64pF/mm²***

On-Chip Capacitor

- Device and MIM capacitors are evaluated
- Targeting area beneath wire bond pad, which is typically unused.



0.1um BPTM Process

- **Device-Based Capacitor : *13 fF/um²***
- **MIM-Based Capacitor : *1.1 fF/um²***

Wire Bond Modeling

- Typical VLSI wire bond lengths range from 1mm to 5mm
- Electrical parameter extraction is used to find L and C or wire bond

Length	L	C	Z_0
1mm	0.569nH	26fF	148Ω
2mm	1.138nH	52fF	148Ω
3mm	1.707nH	78fF	148Ω
4mm	2.276nH	104fF	148Ω
5mm	2.845nH	130fF	148Ω

References

- Radio Frequency Integrated Circuit Design John (Rogers,Calvin Plett)

Budapest University of Technology and Economic
Department of Electron Devices

Circuit Environment

Lecture 8

Signal Integrity

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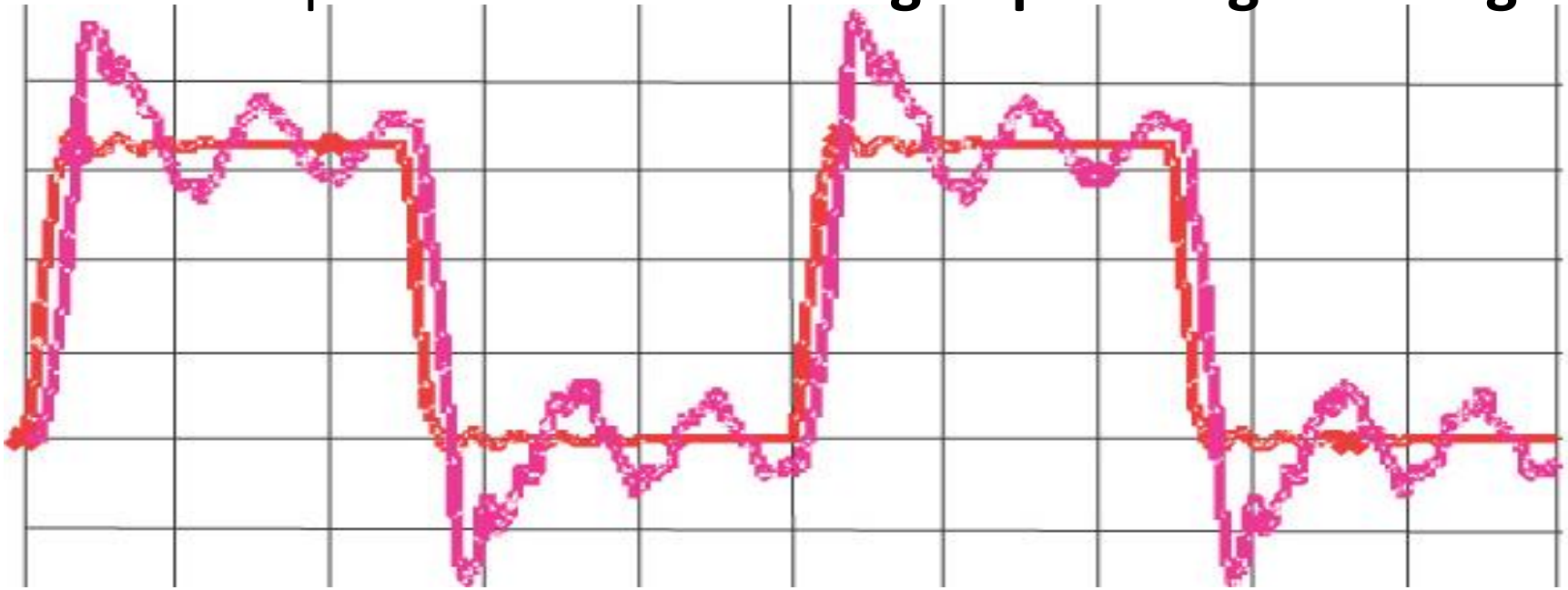
2021/2022

There are two kinds of engineers:
Those who have signal-integrity problems and those who will. **Eric Bogatin**

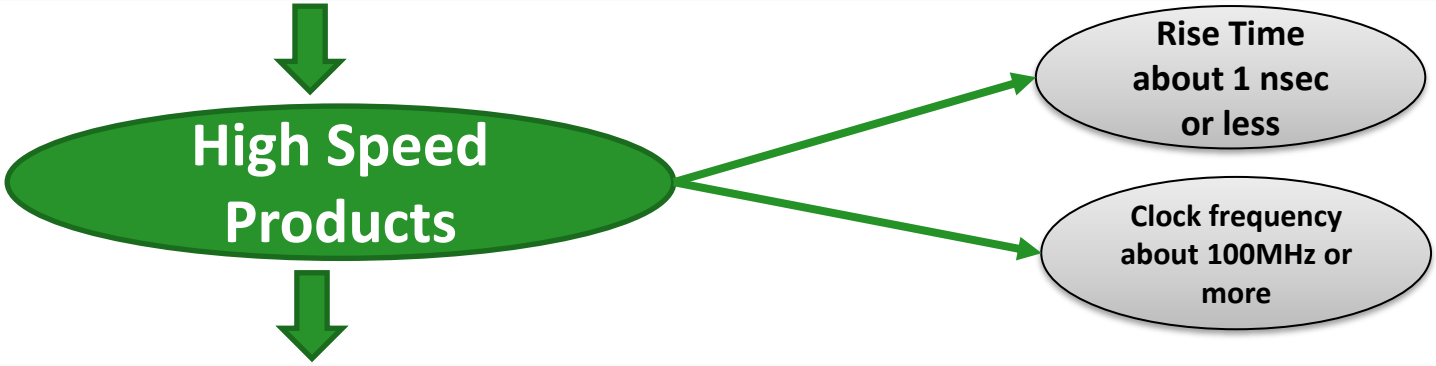
- **Signal Integrity (SI)** is the ability of a system to transfer (data) signals without excessive distortion.
- **SI** is an important concern in **High-Speed Digital Design**



- All engineers who touch a product should have an understanding of how what they do may influence the performance of the overall product.
- By understanding the essential principles of signal integrity at **an intuitive** and **engineering** level,
- Every engineer involved in the design process can evaluate the impact of his/her decisions on system performance.
- This lecture is about the essential principles needed to understand **signal integrity problems and their solutions.**
- The engineering discipline required to deal with these problems is presented at **an intuitive level and a quantitative level**.

What are SI, PI and EMC

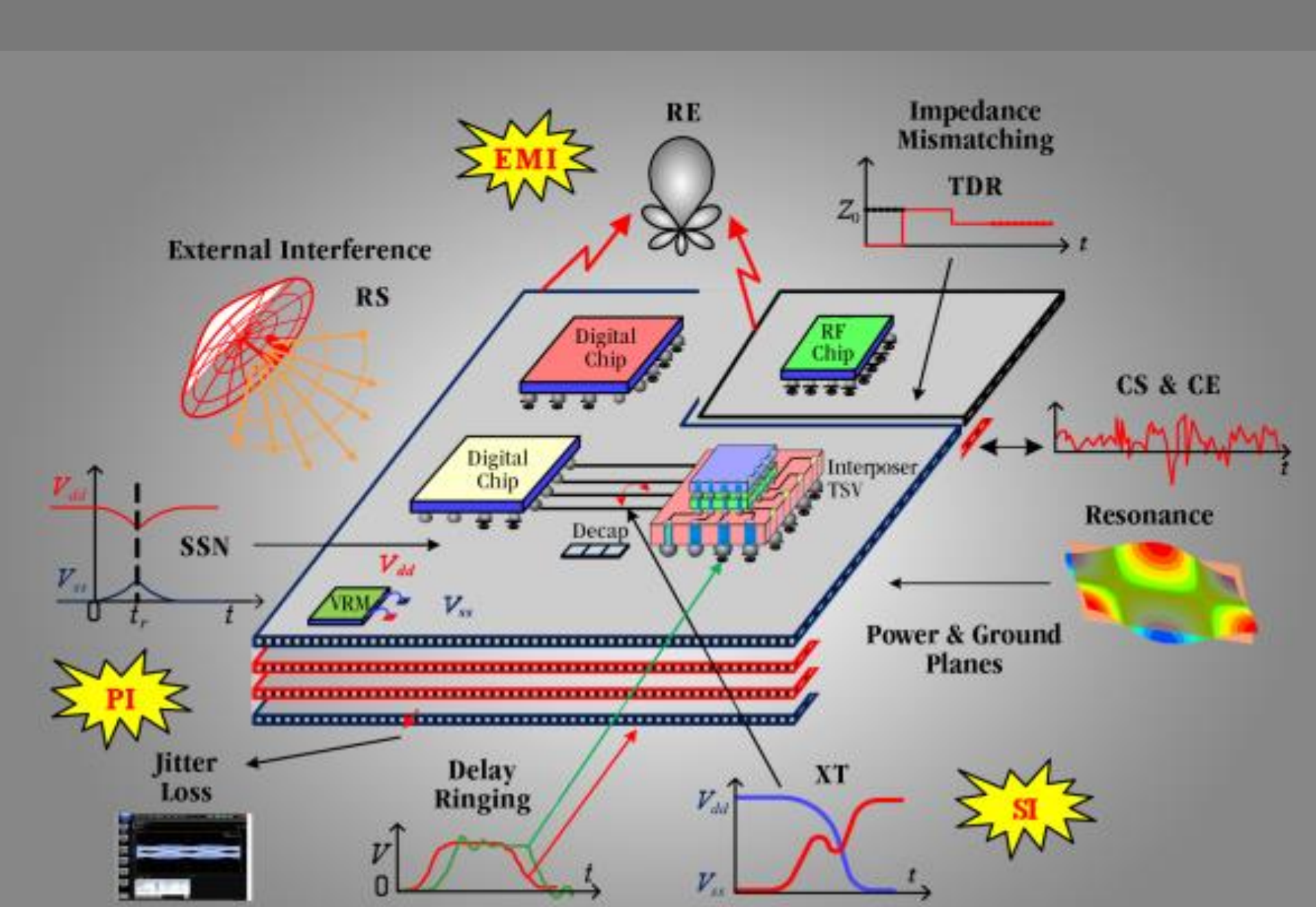
For most electronic products, signal-integrity effects begin to be important at clock frequencies above about 100 MHz or rise times shorter than about 1 nsec.



how the electrical properties of the interconnects, interacting with the digital signal's voltage and current waveforms, can affect performance.

1. **Signal integrity (SI)**, involving the distortion of signals.
2. **Power integrity (PI)**, involving the noise on the interconnects and any associated components delivering power to the active devices.
3. **Electromagnetic compatibility (EMC)**, the contribution to radiated emissions or susceptibility to electromagnetic interference from fields external to the product

In the design process, all three of these electrical performance issues need to be considered for a successful product.



Modeling and Design of Electromagnetic Compatibility for High-Speed Printed Circuit Boards and Packaging (*Xing-Chang Wei)*

Electromagnetic compatibility (EMC)

- The general area of EMC really encompasses solutions to two problems:

1. Too much radiated emission from a product into the outside world
2. Too much interference on a product from radiation coming from the outside world.

- EMC is about engineering solutions for the product so it will at the same time maintain radiated emissions below **the acceptable limit** and **not be susceptible to radiation from the external world**.
- Designing for acceptable EMC involves good SI and PI design as well as additional considerations, especially related to cables, connectors, and enclosure design.
- Spread spectrum clocking (SSC), which purposely adds **jitter** to clocks by modulating their clock frequency, is specifically used to pass an **EMC certification test**.

About jitter

- Jitter: variations in the **timing** of the signal
  - Signal is sampled at defined bit times
  - Signal transitions must occur between sample times
  - Can cause undefined or incorrect values at sample times
    - Creates bit errors
- Many different types of jitter:
  - Data dependent jitter
  - Periodic jitter
  - Random jitter
  - etc.

Power integrity (PI)

- PI is about the problems associated with the power distribution network (PDN), which includes all the interconnects **from the voltage regulator modules (VRMs) to the voltage rail distributed on the die.** This includes:

1. The power and ground planes in the board and in the packages,
2. The vias in the board to the packages,
3. The connections to the die pads,
4. Any passive components like capacitors connected to the PDN.

- Since the PDN that feeds the on-die core power rail, sometimes referred to as the *Vdd rail*, is exclusively a PI issue,
- So, there are many overlapping problems between PI and SI topics.
- This is primarily because the **return paths** for the signals use the same interconnects usually associated with the PDN interconnects, and anything that affects these structures has an impact on both **signal quality** and **power quality.**

Note:

The overlap between PI and SI problems adds confusion to the industry because problems in this gray area are either owned by two different engineers or fall through the cracks as the PI engineer and the SI engineer each think it's the other's responsibility.

Signal integrity (SI)

- In the SI domain, problems generally relate to either:

1. Noise issues
2. Timing issues,

- Each of which can cause **false triggering** or **bit errors** at the receiver.

Timing issues

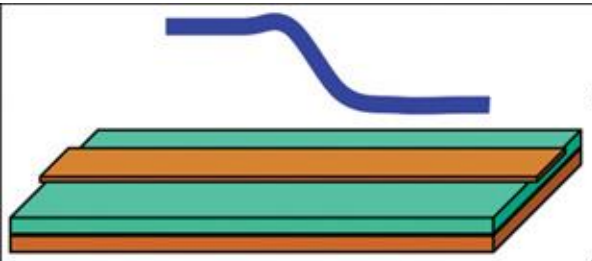
- Timing is a complicated field of study. In one cycle of a clock, a certain number of operations must happen.
- This short amount of time must be divided up and allocated, in a budget, to all the various operations. For example, some time is allocated:

1. For gate switching,
2. For propagating the signal to the output gate,
3. For waiting for the clock to get to the next gate,
4. For waiting for the gate to read the data at the input.

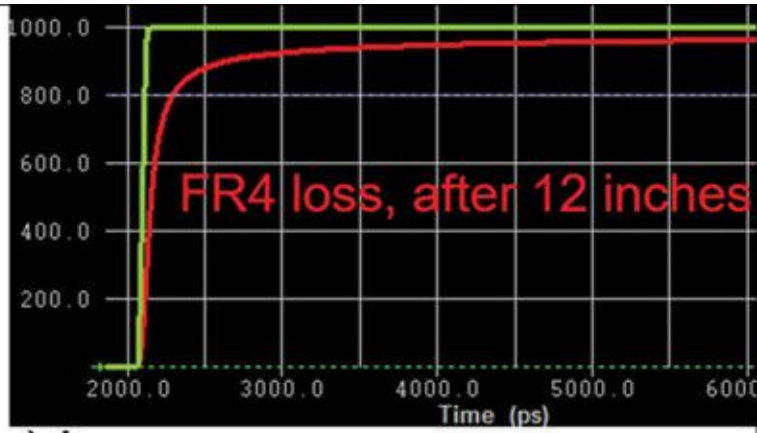
- **Though the interconnects affect the timing budget,**

Signal-Integrity noise problems

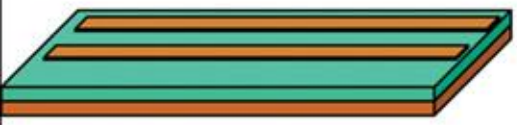
Classify every SI/PI/EMC problem into one of these six families.



1. Reflection noise

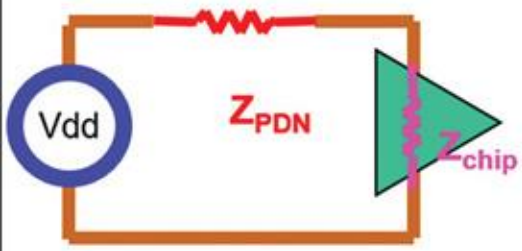


2. Cross talk



3. Ground (and power) bounce

4. Losses (@ Gbps)



5. Rail collapse, voltage droop, power supply noise

6. EMI

Keep in your Mind

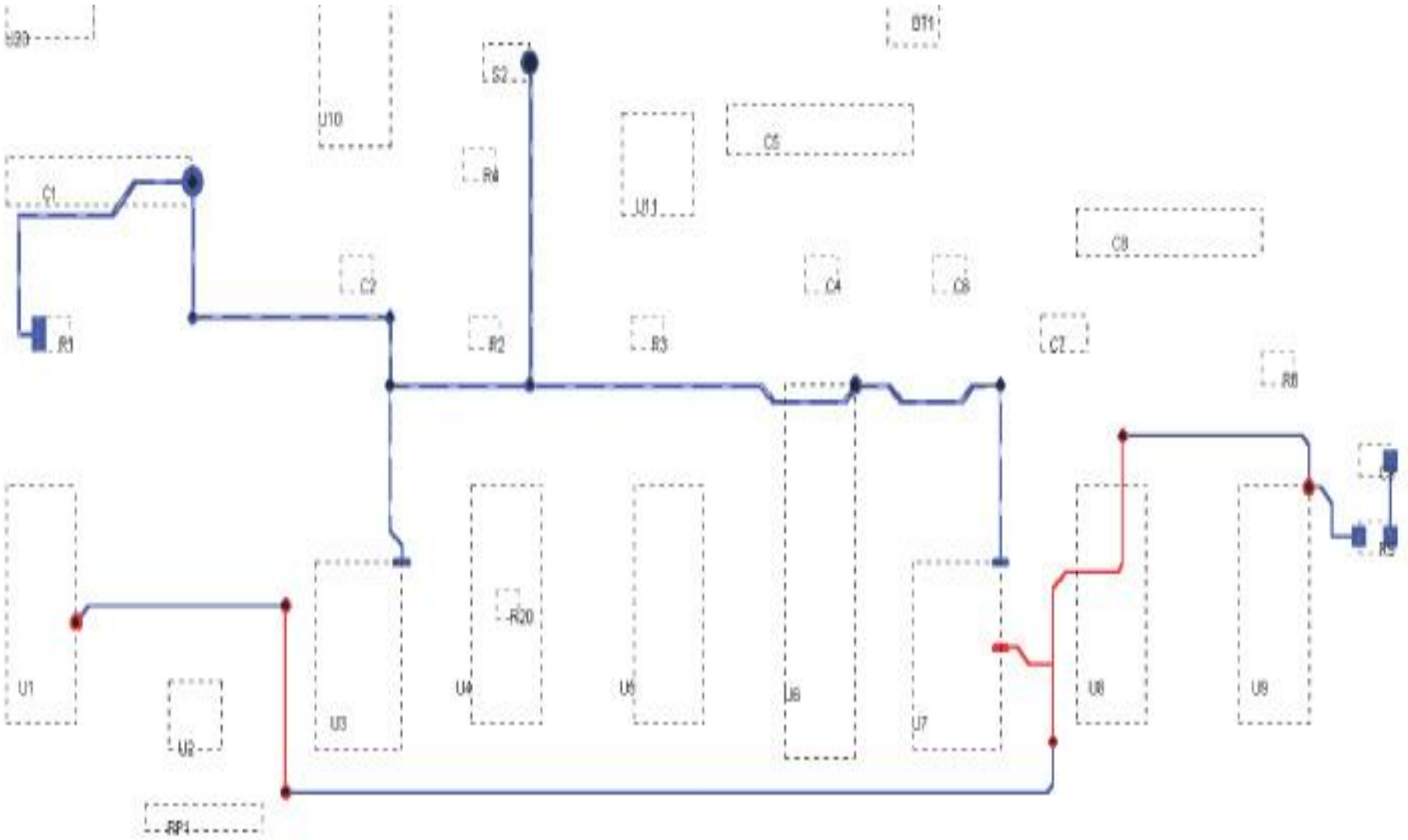
- These problems play a role in all interconnects, from the smallest on-chip wire to the cables connecting racks of boards and everywhere in-between.
- The essential principles and effects are the same.
- The only differences in each physical structure are the specific **geometrical feature sizes** and **the material properties.**

SIGNAL-INTEGRITY EFFECTS ON ONE NET

- A net is made up of all the metal connected together in a system.
- There are three common problems associated with signals on a single net being distorted by the interconnect.

1. Reflections. **[The only thing that causes a reflection is a change in the instantaneous impedance the signal encounters].**
2. Frequency-dependent losses in the line from the conductor and the dielectric.
3. Timing. [**The time delay difference between two or more signal paths is called skew. When a signal and clock line have a skew different than expected, false triggering and errors can result].**

SIGNAL-INTEGRITY EFFECTS ON ONE NET.



Reflections

- The instantaneous impedance the signal sees depends as much on the physical features of **the signal trace as on the return path.**
- If there are enough impedance changes, the distortions can cause **false triggering.**
- Some of the features that would change the impedance the signal sees include the following:

1. An end of the interconnect
2. A line-width change
3. A layer change through a vias
4. A gap in return-path plane
5. A connector
6. A routing topology change, such as a branch, tee, or stub

Reflections

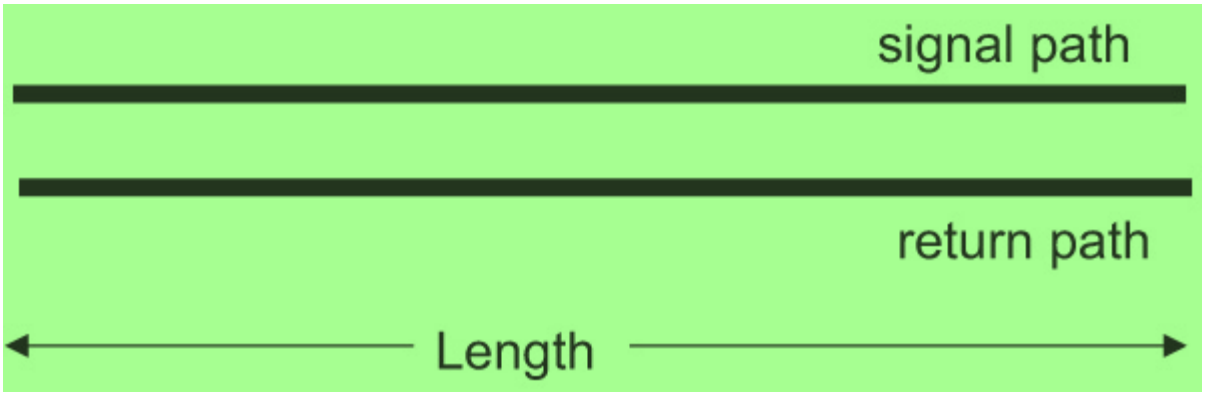
The way to minimize the problems associated with impedance changes is to keep the instantaneous impedance the signal sees constant throughout the net.

- This strategy is typically implemented by following four best design practices:

1. Use a board with constant, or "controlled," impedance traces. This usually means using uniform transmission lines.
2. To manage the reflections from the ends, use a termination strategy that controls the reflections by using a resistor to fool the signal into not seeing an impedance change.
3. Use routing rules that allow the topology to maintain a constant impedance down the trace.
4. Engineer the structures that are not uniform transmission lines to reduce their discontinuity. This means adjusting fine geometrical design features to carve the fringe fields.

The Physical Basis of Transmission Lines

- **Transmission line** is composed of any two conductors that have length.
- **Transmission line** is used to transport a signal from one point to another.



- **Transmission line** has two very important parameters: a characteristic impedance (ohm) and a time delay (second).

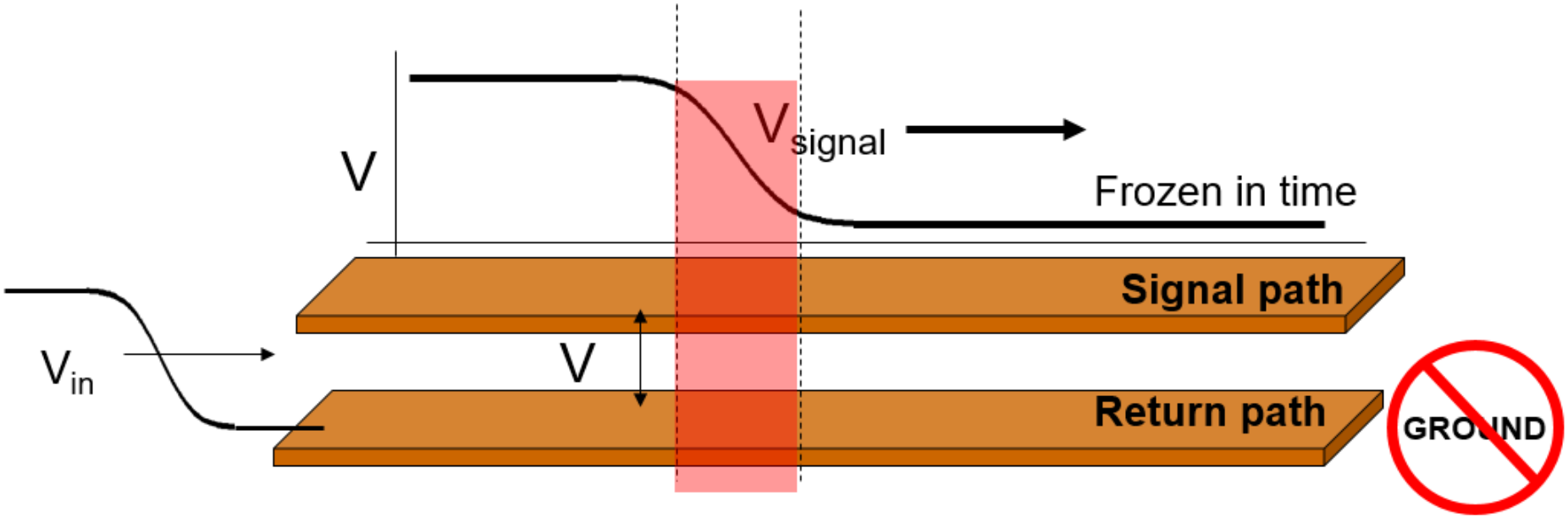
FORGET THE WORD *GROUND*

- The term ***ground*** is reserved for the conductor with the lowest voltage in the circuit compared to any other node in the circuit.
- Using the term **ground** to refer to the **return path** is a very bad habit and should be avoided.
- It is much healthier to get into the habit of calling the other conductor the ***return path.***
- Many of the problems related to **signal integrity** are due to poorly designed return paths.

When we label the other path as ground, we typically think it is a universal sink for current. Return current goes into this connection and comes out wherever there is another ground connection.
This is totally wrong.

THE SIGNAL

- When a signal moves down a transmission line, it simultaneously uses **the signal path and the return path**.
- **Both conductors** are equally important in determining how the signal interacts with the interconnect.
- When a signal is launched into a transmission line, it propagates down the line at **the speed of light in the material.**

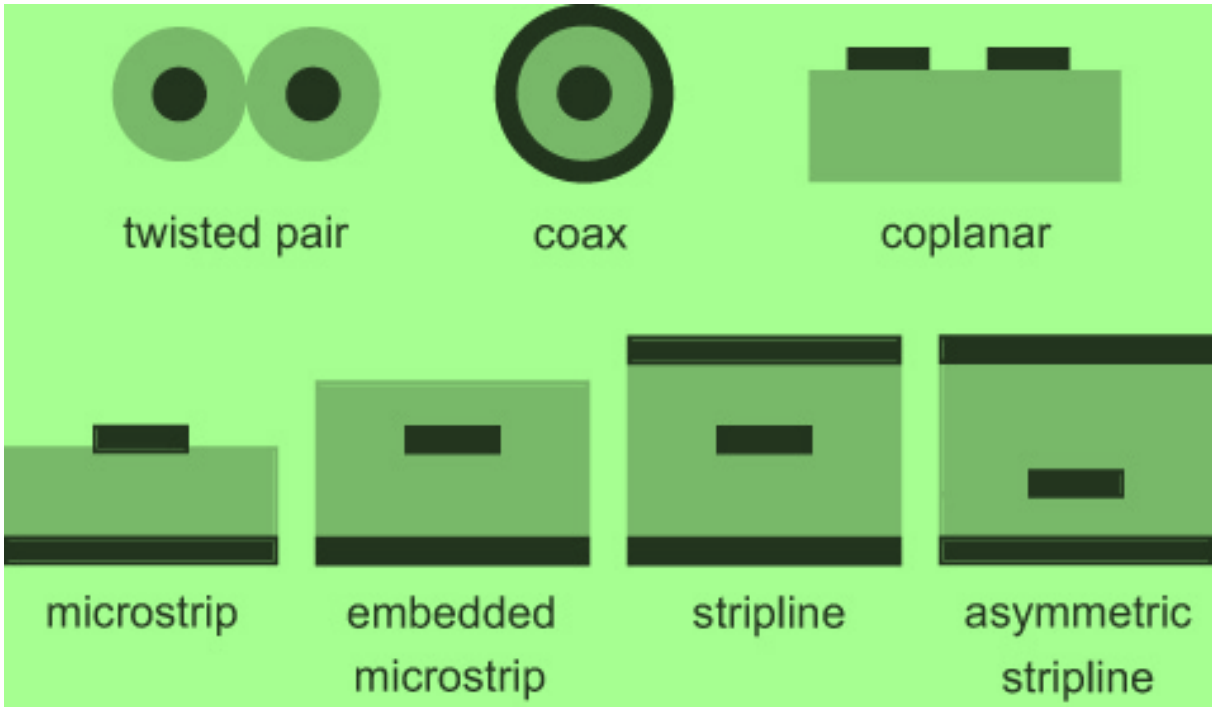


UNIFORM TRANSMISSION LINES.

- Classify transmission lines by their geometry.
- The **uniformity** of the **cross section** down its length.=> uniform OR nonuniform.

Reflections will be minimized and signal quality optimized if the transmission lines are uniform or are controlled impedance. All high-speed interconnects should be designed as uniform transmission lines.

- The **identical** of each of its two conductors.



Keep in your Mind

In general, for most transmission lines, the signal quality and cross-talk effects will be completely unaffected by whether the line is balanced or unbalanced. However, ground-bounce and EMI issues will be strongly affected by the specific geometry of the return path.

Whether the transmission line is uniform or nonuniform, balanced or unbalanced, it has just one role to play: to transmit a signal from one end to the other with an acceptable level of distortion.

How fast do signals travel down a transmission line?

- Is the speed of a signal the same **THE SPEED OF ELECTRONS IN WIRE!!!**

- **If reducing the resistance of the interconnect will increase the speed of a signal!!!**

- **In fact, the speed of the electrons in a typical copper wire is actually about 10 billion times slower than the speed of the signal.**

The speed of an electron in a copper wire?

$$I = \frac{\Delta Q}{\Delta t} = \frac{q \times n \times A \times v \times \Delta t}{\Delta t} = q \times n \times A \times v$$

$$v = \frac{I}{q \times n \times A}$$

where:

I = current passing one point, in Amps

ΔQ = charge flowing in a time interval, in Coulombs

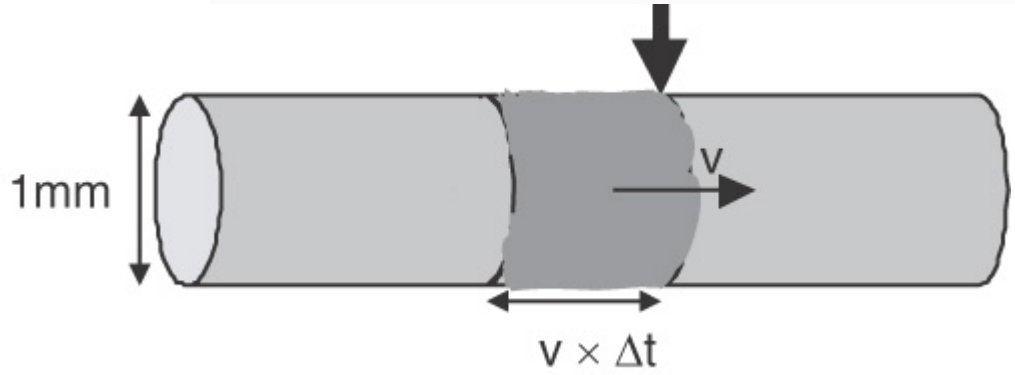
Δt = time interval

q = charge of one electron = 1.6×10^{-19} Coulombs

n = density of free electrons, in $\#/m^3$

A = cross-sectional area of the wire, in m^2

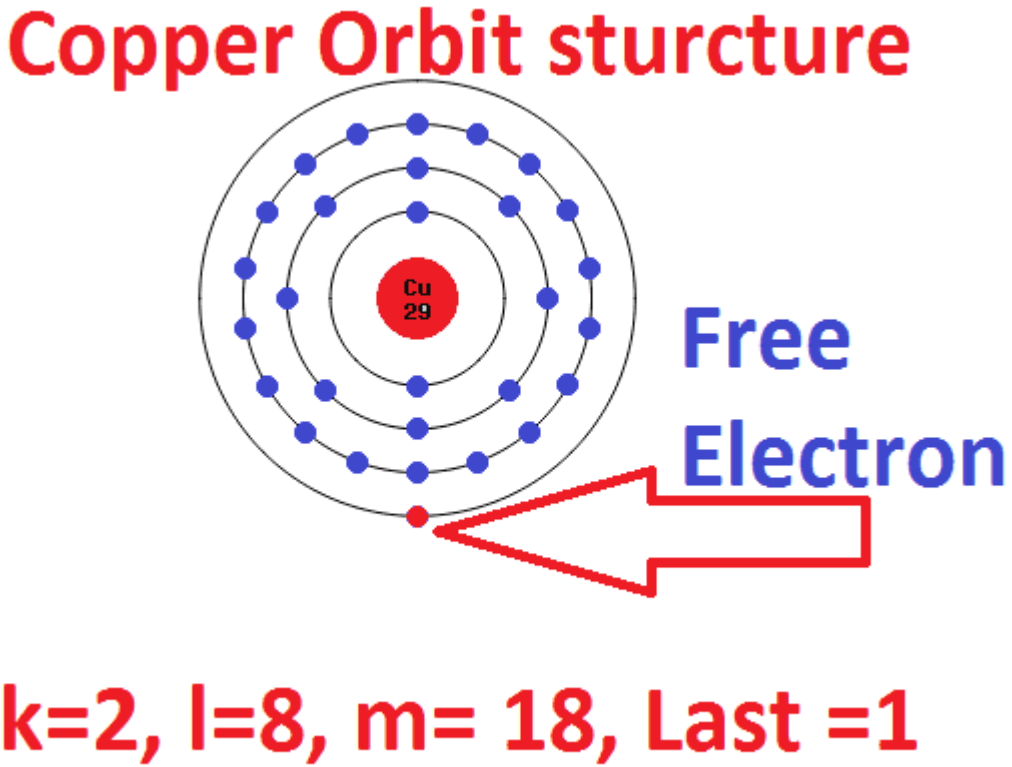
v = speed of the electrons in the wire, in m/sec



The speed of an electron in a copper wire?

$$v = \frac{I}{q \times n \times A} = \frac{1\,\text{Amp}}{10^{-19} \times 10^{27} \times 10^{-6}} = 10^{-2}\,\frac{\text{m}}{\text{sec}} = 1\,\frac{\text{cm}}{\text{sec}}$$

- An electron travels at a speed of about 1 cm/sec. This is about as fast as an ant walks on the ground.



How signal transfer at speed of light?

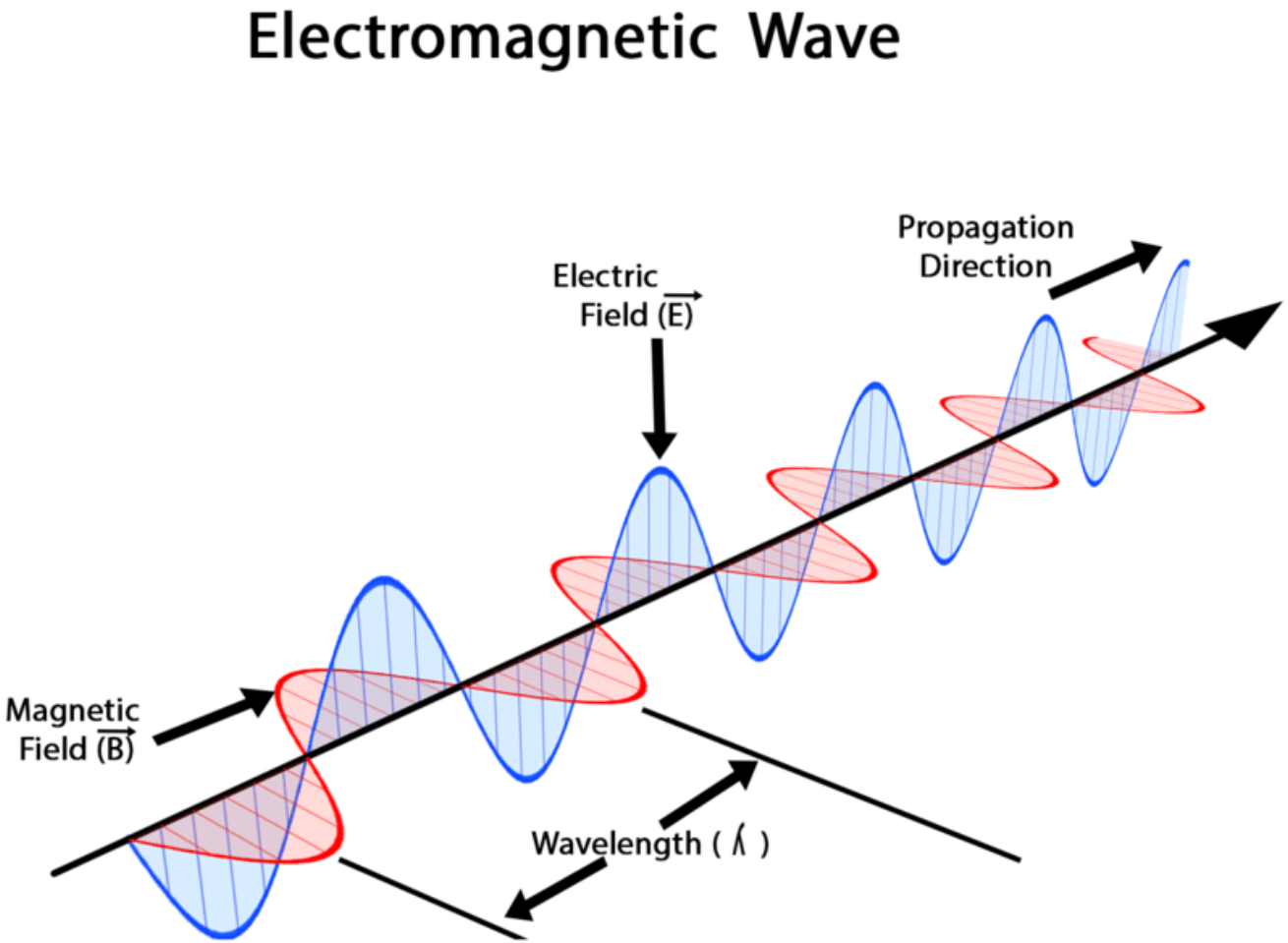
- When **one electron** in a wire is jiggled by the source, its interaction with the adjacent electron through the **electric field** between them jiggles.
- This *kink* in the electric field propagates to the next electron at the speed of light allowed by the changing field.
- **The kinks** in the electric field between the electrons-that determines how fast this signal propagates, **not the speed of the electrons themselves.**

Keep in your mind

The speed of a signal depends on the materials that surround the conductors and how quickly the changing electric and magnetic fields associated with the signal can build up and propagate in the space around the transmission line conductors.

Electromagnetic Wave

- Electromagnetic Waves - YouTube



References

- **Signal and Power Integrity - Simplified by Eric Bogatin.**
- **FUNDAMENTALS OF APPLIED ELECTROMAGNETICS by Fawwaz T. Ulaby**

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Lecture 9

Signal Integrity II

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2021/2022

How signal transfer at speed of light?

- When **one electron** in a wire is jiggled by the source, its interaction with the adjacent electron through the **electric field** between them jiggles.
- This *kink* in the electric field propagates to the next electron at the speed of light allowed by the changing field.
- **The kinks** in the electric field between the electrons-that determines how fast this signal propagates, **not the speed of the electrons themselves.**

Keep in your mind

The speed of a signal depends on the materials that surround the conductors and how quickly the changing electric and magnetic fields associated with the signal can build up and propagate in the space around the transmission line conductors.

How signal transfer at speed of light?

- This kink of field will propagate through the dielectric material surrounding the transmission line **at the speed of a changing electric and magnetic field**, which is the speed of light in the material.
- How quickly **the electric and magnetic fields** can build up is what really determines the **speed of the signal.**
- The propagation and interaction of these fields is described by **Maxwell's Equations**.

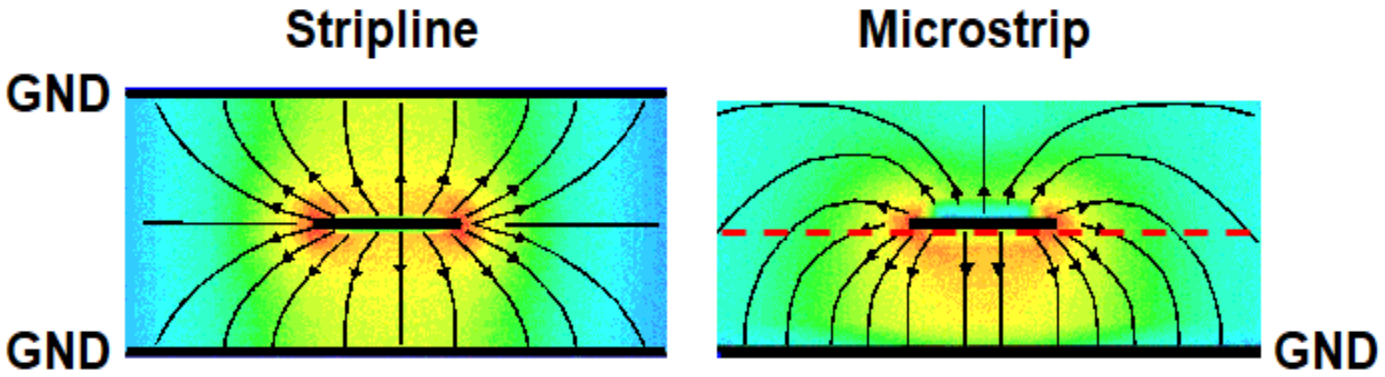
$$v = \frac{1}{\sqrt{\varepsilon_0 \varepsilon_r \mu_0 \mu_r}}$$

- All polymers that do not contain a ferromagnetic material have a magnetic permeability of 1. Therefore, this term can be ignored.

$$u_p = \frac{c}{\sqrt{\epsilon_r}},$$

Electric Field sees

- In the case of stripline, for example, all the fields see the same material, and the effective dielectric constant is the bulk dielectric constant.
- when the field lines see a combination of dielectric materials, as in a microstrip where there are some field lines in the bulk material and some in the air above, the effective dielectric constant that affects the signal speed is a combination of the different materials.



https://www.nwengineeringllc.com/article/how-low-are-dielectric-losses-in-microstrip-lines.php

Time Delay:

$$TD = \frac{Len}{v}$$

- **Wiring Delay** is the duration of time that the data signal takes to propagate from one point in the transmission line to another.
- It is the reciprocal of propagation speed.

$$t_{PD} = \frac{\sqrt{\varepsilon_r}}{c}$$

- Example: For FR4 (is the most common grade dielectric material that is used in the fabrication of circuit boards), **what is wiring delay? ε_r=4.**

BE THE SIGNAL:

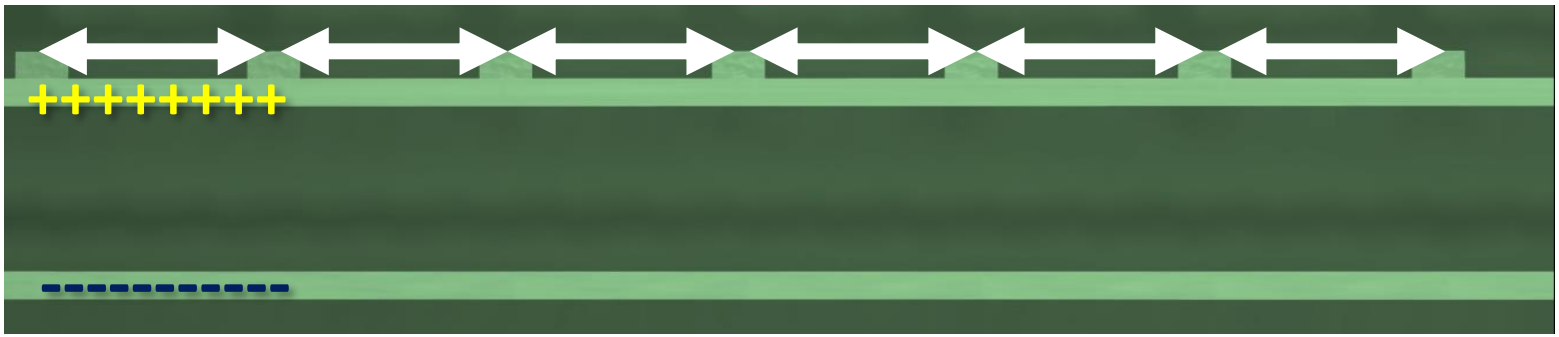
- All a signal cares about is how fast it moves down the line and what impedance it sees.
- speed is based on the material properties of the dielectric and their distribution.
- We'll make it 10 feet long, so that we can actually walk down it and, "be the signal" to observe what the signal would see.

What impedance do we see?

- We will answer this question by determining the ratio of the voltage applied, 1 v, and the current coming out of our foot to drive the signal down the transmission line.
- Launch a signal into one end by connecting a 1-v battery between the two conductors at the front end.
- **At the initial instant** that we have launched the signal into the line, there has not been enough time for the signal to travel very far down the line.

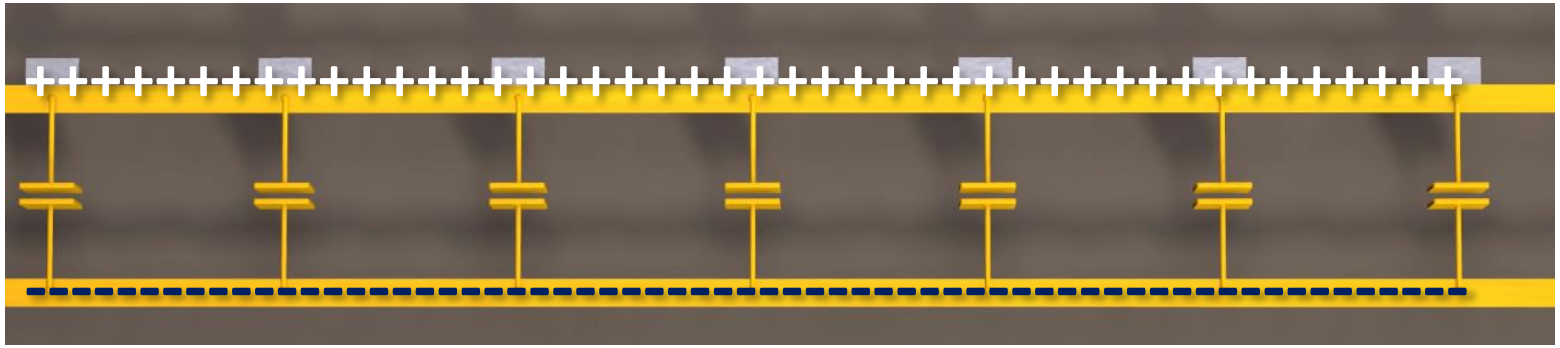
BE THE SIGNAL CONT.:

- Let’s assume that the speed of propagation is 1 foot per nsec.
- After the first nsec, the voltage on the far end of the line is still zero
- As the signal hasn’t had enough time to get very far.
- The signal along the line would be about 1 volt for the first foot and zero for the remaining length of the line.
- Let’s freeze time after the first nsec and look at the charges on the line.
- There will be a 1-volt difference.



BE THE SIGNAL CONT.:

- We know that because the signal and return paths are two separated conductors.
- There are some capacitance between the conductors in this region.
- If there is a 1-v difference between them, there must also be some charge on the signal conductor and an equal and opposite amount on the return-path conductor.
- In the next 1 nsec:



BE THE SIGNAL CONT.:

- The fact that the signal is propagating down the line means that the capacitance between the signal and return paths is getting charged up.
- **What is the current that must flow to charge up successive regions of the transmission line as the signal propagates?**
- If the transmission line has the **same capacitance per length**. Then?
- If the signal travels in **transmission line at fixed speed**. Then?

What affects the current coming out of our foot to charge up the line?

$$I \sim v \times C_L$$

What is the impedance of the line?

- The basic definition of *impedance* of any element is the ratio of voltage applied to current through it.
- For each step we must ask: ***What is the ratio of the voltage applied to the current being injected into the line?***
- The voltage of the signal is fixed at the signal voltage.
- The current into the line depends on the capacitance of each footstep and how long it takes to charge up each footstep.
-

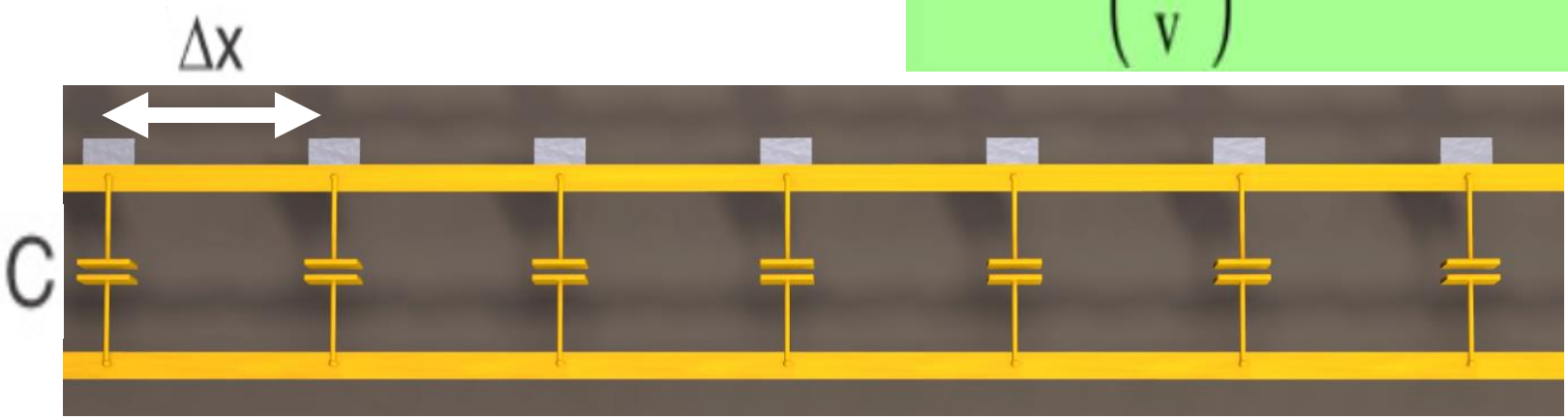
As long as the speed of the signal is constant and the capacitance of each footstep is constant, the current injected into the line by our foot will be constant, and the impedance of the line the signal sees will be constant.

Zeroth-order model of a transmission line:

- This is the defining relationship for the current voltage (I-V) behavior of a transmission line.
- It says the instantaneous current of a signal anywhere on a transmission line is directly proportional to the voltage.
- Double the voltage applied, and the current into the transmission line will double. This is exactly how a resistor behaves.

$$C = C_L \times \Delta x$$

$$I = \frac{Q}{\Delta t} = \frac{CV}{\left(\frac{\Delta x}{v}\right)} = \frac{C_L \Delta x v V}{\Delta x} = C_L v V$$



The instantaneous impedance:

- The instantaneous impedance a signal sees depends on only two terms, both of which are intrinsic to the line.
- It doesn't depend on the length of the line.
- The instantaneous impedance of the line depends on the cross section of the line and the material properties.
- As long as these two terms are constant as we move down the line, a signal would see the same constant, instantaneous impedance.
- The unit of instantaneous impedance of the line is Ohms, as with any impedance.
- Example: the dielectric constant is 4 and the capacitance per length of the line is 130 pF/m, find Z

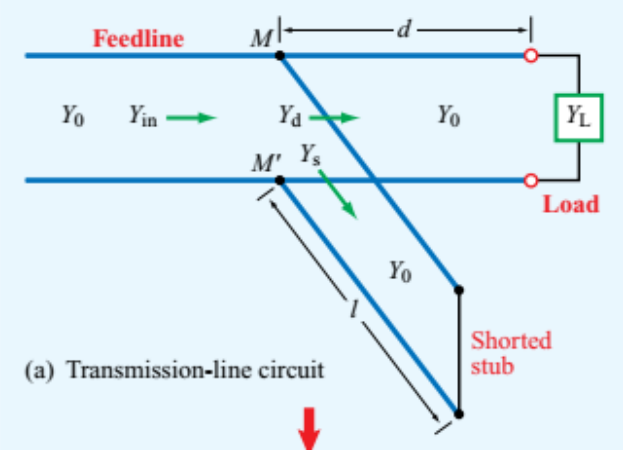
$$Z = \frac{V}{I} = \frac{V}{C_L v V} = \frac{1}{C_L v}$$

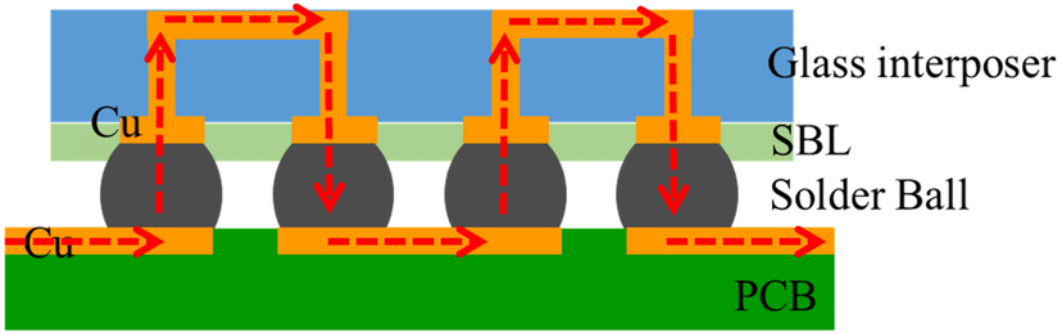
WHY ARE THERE REFLECTIONS?

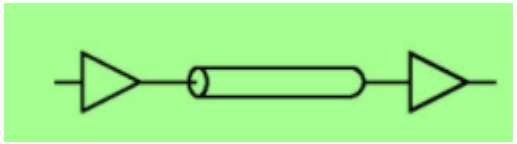
- Reflections occur whenever the instantaneous impedance the signal sees changes.
- This can be at the ends of lines or wherever the topology of the line changes, such as at **corners, vias, branches, connectors**, and **packages**.

For optimal signal quality, the goal in interconnect design is to keep the instantaneous impedance the signal sees as constant as possible.

- To keep the instantaneous impedance constant: there are various methods such as: **minimizing stub lengths, using daisy chains rather than branches, and using point-to-point topology.**







REFLECTIONS AT IMPEDANCE CHANGES:

- As a signal propagates down a transmission line,
- It sees an instantaneous impedance for each step along the way.
- If the interconnect is a controlled impedance, then the instantaneous impedance will be constant and equal to **the characteristic impedance** of the line.
- If the instantaneous impedance ever changes, for whatever reason, some of the signal will **reflect back** in the opposite direction, and some of it will continue with a **different amplitude**.
- We call all locations where the instantaneous impedance changes ***impedance discontinuities* or just *discontinuities*.**
- The amount of signal that reflects depends on the magnitude of the change in the instantaneous impedance.

$$\frac{V_{reflected}}{V_{incident}} = \frac{Z_2 - Z_1}{Z_2 + Z_1} = \rho$$

How to minimize signal-integrity problems?

1. Use controlled impedance interconnects.

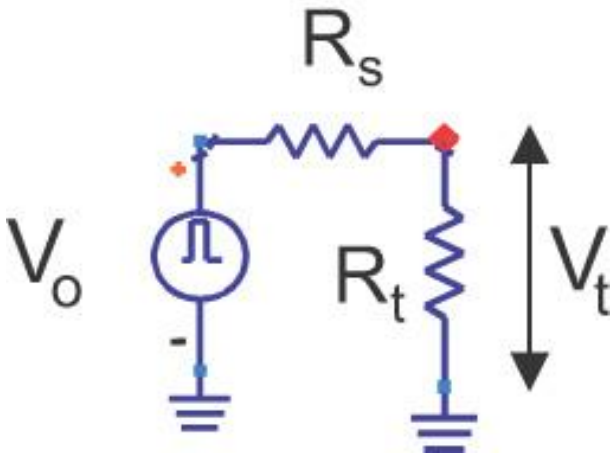
2. Provide at least one termination at the ends of a transmission line.

3. Use a routing topology that minimizes the impact from multiple branches.

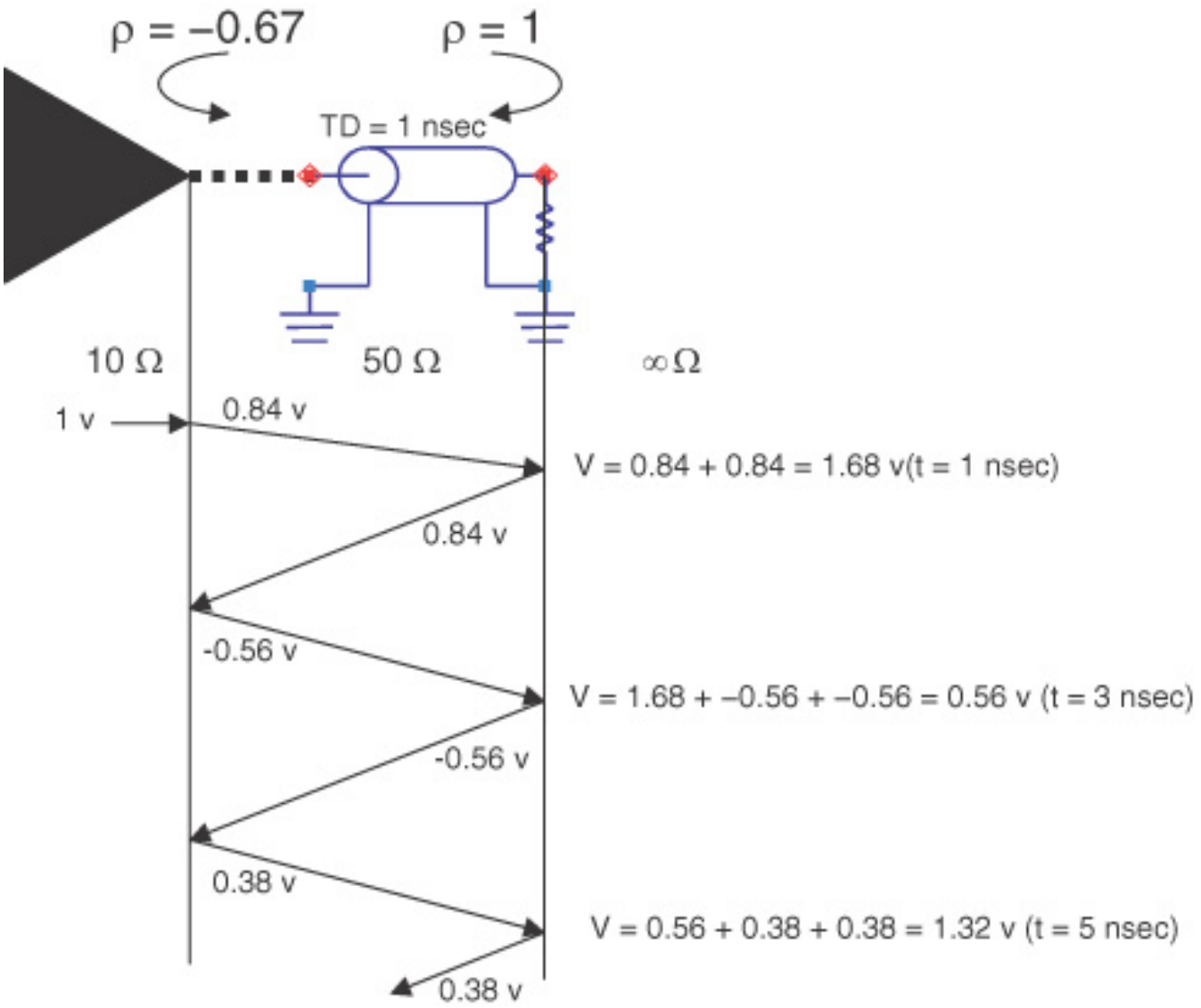
4. Minimize any geometry discontinuities.

SOURCE IMPEDANCE:

- When a signal is launched into a transmission line, there is always some impedance of the source.
- For typical CMOS devices, this can be about 5 Ohms to 20 Ohms.
- For older-generation transistor-transistor logic (TTL) gates, this can be as high as 100 Ohms.

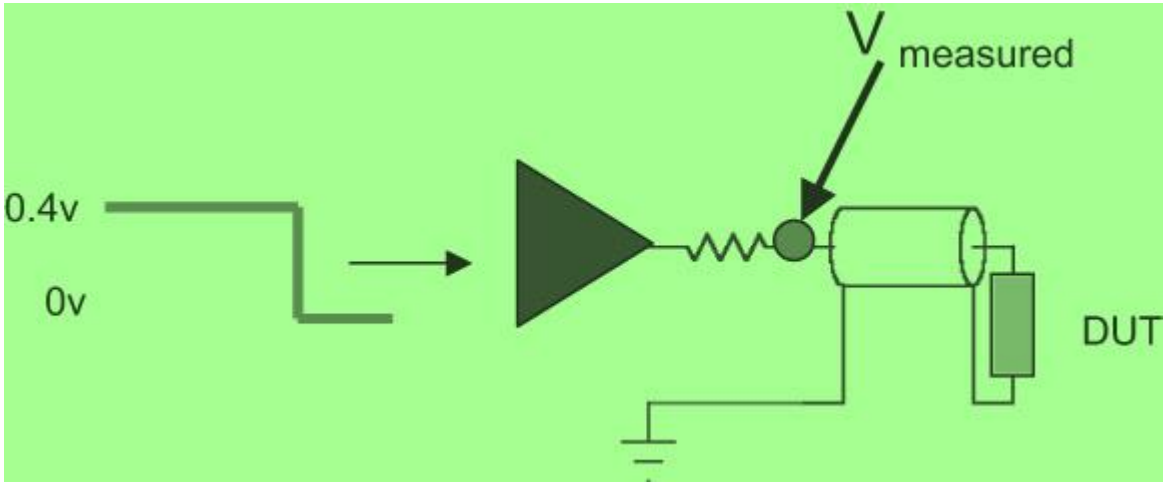


BOUNCE DIAGRAMS:



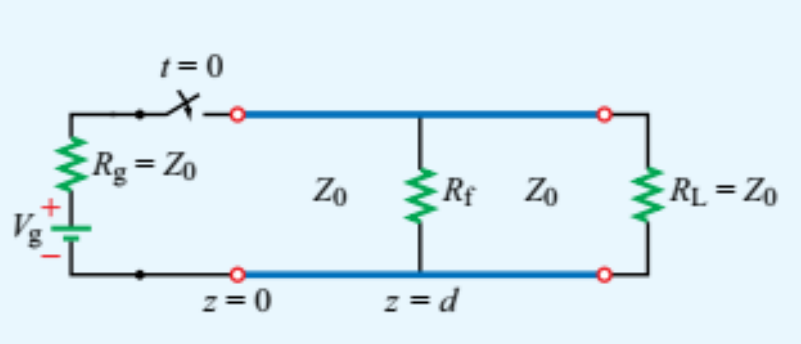
MEASURING REFLECTIONS WITH A TDR:

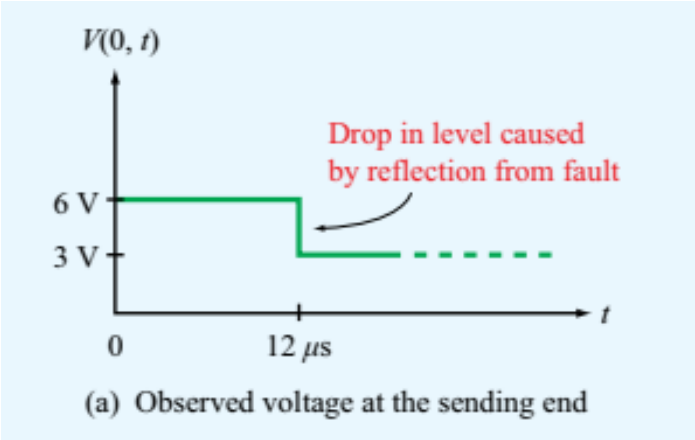
- *Time-Domain Reflectometer* (*TDR*).
- A time-domain reflectometer (TDR) is an instrument used to locate faults on a transmission line.
- A TDR sends a step voltage down the line, and by observing the voltage at the sending end as a function of time.
- A TDR will generate a short rise-time step edge, typically between 35 psec and 150 psec,



Example:

- If the voltage waveform shown in below is seen on an oscilloscope connected to the input of **a 75 matched transmission line**, determine (a) the generator voltage, (b) the location of the fault, and (c) the fault shunt resistance. The line's insulating material is Teflon with r = 2.1.



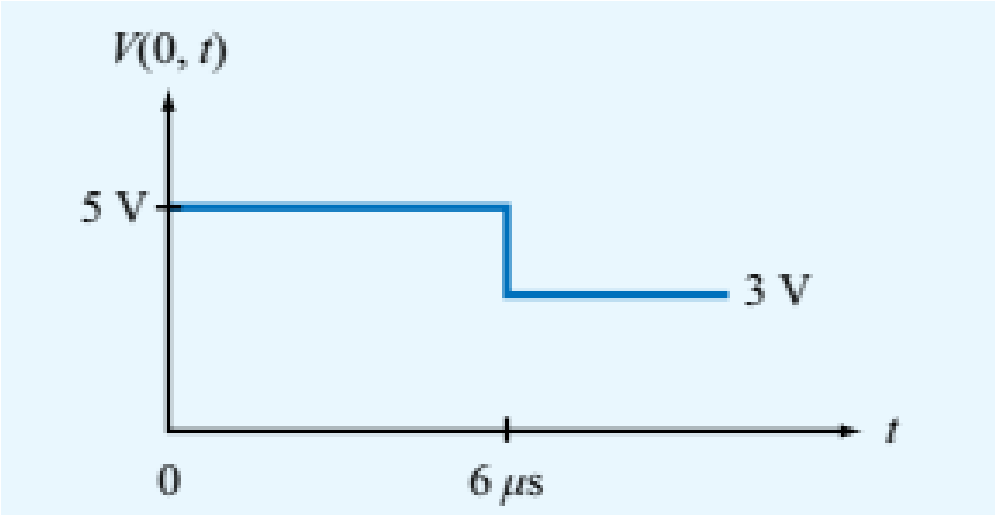


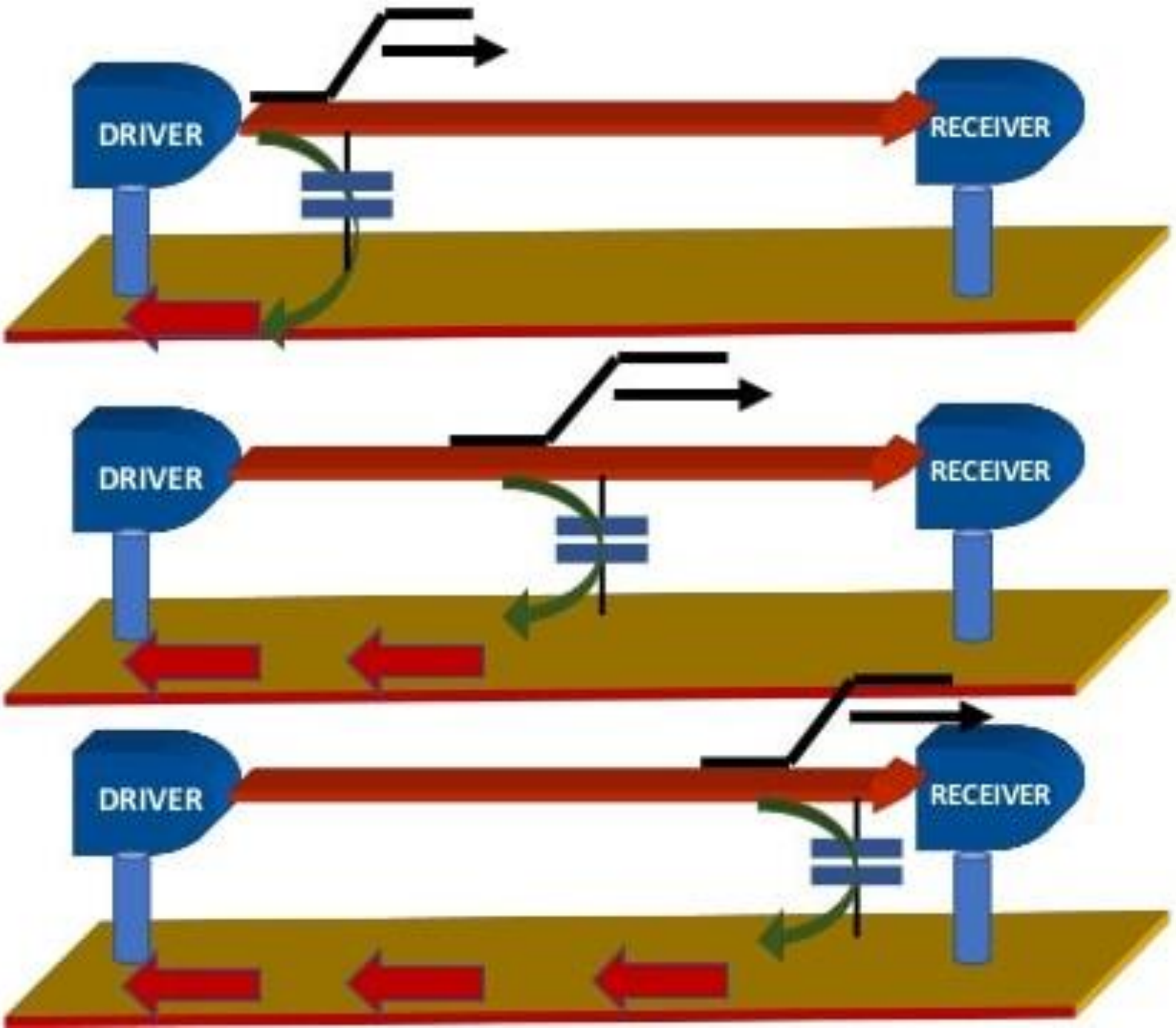
(a) Observed voltage at the sending end

HW:

In response to a step voltage, the voltage waveform shown in Figure below was observed at the sending end of a lossless transmission line with Rg = 50Ω , Z0 = 50 Ω , and ε_r = 2.25.

Determine the following:
(a) The generator voltage.
(b) The length of the line.
(c) The load impedance.

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Lecture 7

Parasitic effects of packaging II

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2021/2022

Packaging Parasitic

- The effects of packaging on RFICs.
- **The effects of packaging on thermal management of ICs**

Importance of Thermal Management

- Thermal management of an electronic system encompasses all the thermal processes and technologies that must be utilized to move and transport heat from individual components to the system thermal sink in a controlled manner.
- **Thermal management has two primary objectives:**

1. To ensure that the temperature of each component is maintained within both its **functional** and **maximum allowable limit**.

   A) The functional temperature limit defines the maximum temperature up to which the electrical circuits may be expected to meet their specified performance targets.

   Result in performance degradation or logic errors ”

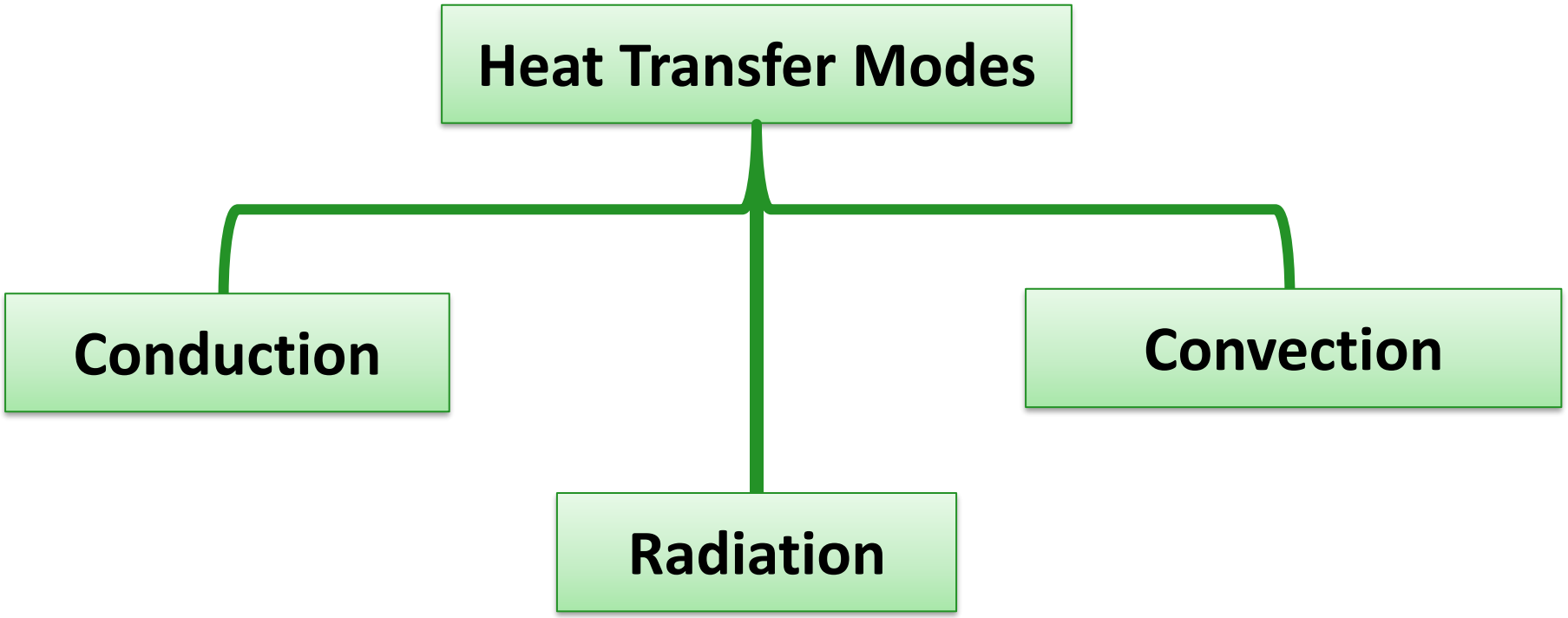
   B) The maximum allowable temperature limit is the highest temperature to which a component or part thereof may be safely exposed.

   May cause irreversible changes in its operating characteristics or may even cause physical destruction of the component “

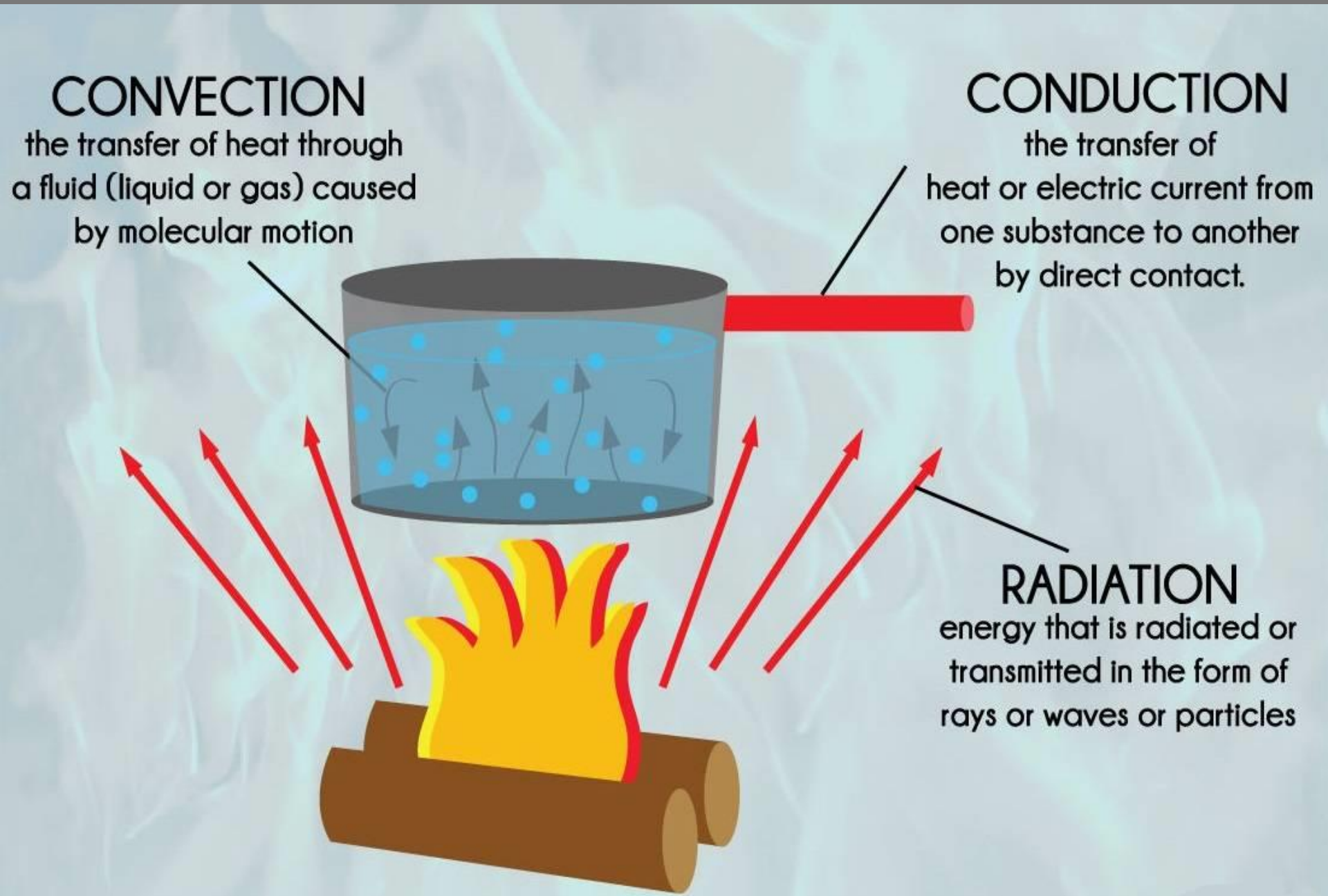
2- To ensure that the temperature distribution in each component satisfies **reliability** objectives.

- **Reliability** is defined as the probability that a device will perform its required function under stated conditions for a specific period of time.
- Failure mechanisms encountered in electronic components are kinetic in nature and depend exponentially on the device operating temperature.
- The exact relationship between the failure rate and temperature depends upon **the thermophysical properties of the packaging materials** and the **failure mechanism in operation.**

- To understand the thermal characteristics of electronic components and packages.
- Heat is transferred from one point to another.
- Three modes:



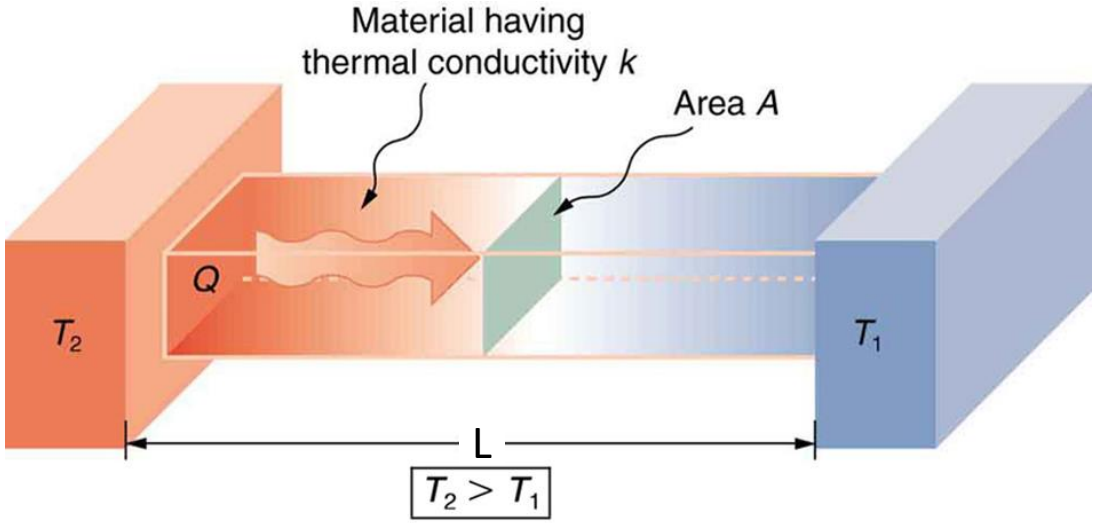
Heat Transfer Modes



Conduction is a mode of heat transfer in which heat flows from a region of higher temperature to one of lower temperature within a medium (solid, liquid, or gaseous) or media in direct physical contact.

$$q = -kA\frac{\Delta T}{L} = -KA\frac{T_1 - T_2}{L}$$

$$q = \frac{\Delta T}{L/kA}$$



Convection is a mode of heat transport from a solid surface to a fluid and occurs due to the bulk motion of the fluid.

$$qc = h_c A(T_s - T_a)$$

$$q_c = \frac{T_s - T_a}{1/h_c A}$$

- **In forced convection, fluid flow is created by an external factor such as a fan.**
- **In free or natural convection, fluid motion is induced by density variations resulting from temperature gradients in the fluid.**

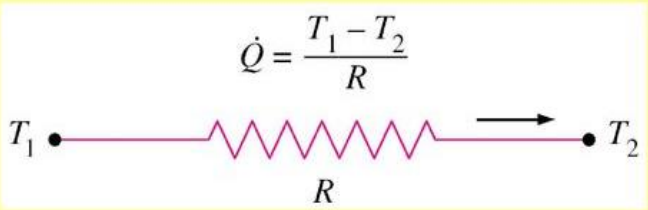
- Radiation heat transfer occurs as a result of radiant energy emitted from a body by virtue of its temperature.
- Radiation heat transport occurs without the aid of any intervening medium.
- Radiant energy is sometimes envisioned to be transported by electromagnetic waves, at other times by photons.

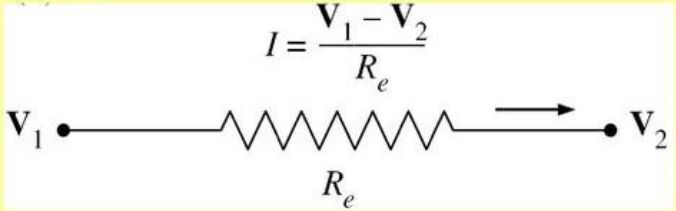
$$q_{rad} = \sigma \varepsilon A_i F_{ij} (T_i^4 - T_j^4)$$

In the case of most low-power electronic applications, these temperature differences are relatively small and, therefore, radiation effects are normally neglected. But for power application, heat transfer by radiation should be considered.

Thermal-electrical analogy: thermal network

Q_t Heat (Joule)	q_t Heat flow rate (J/s)		$1/C_t$ C_t:Thermal capacitance	R_t Thermal resistance	T Temp. (°C)
q Charge (Coulomb)	i Current (Amper)	L Induc. (Henry)	1/C C:Capac. (Farad)	R Resistance (Ohm)	V Voltage (Volt)





Heat Transfer ↔ Electrical current flow

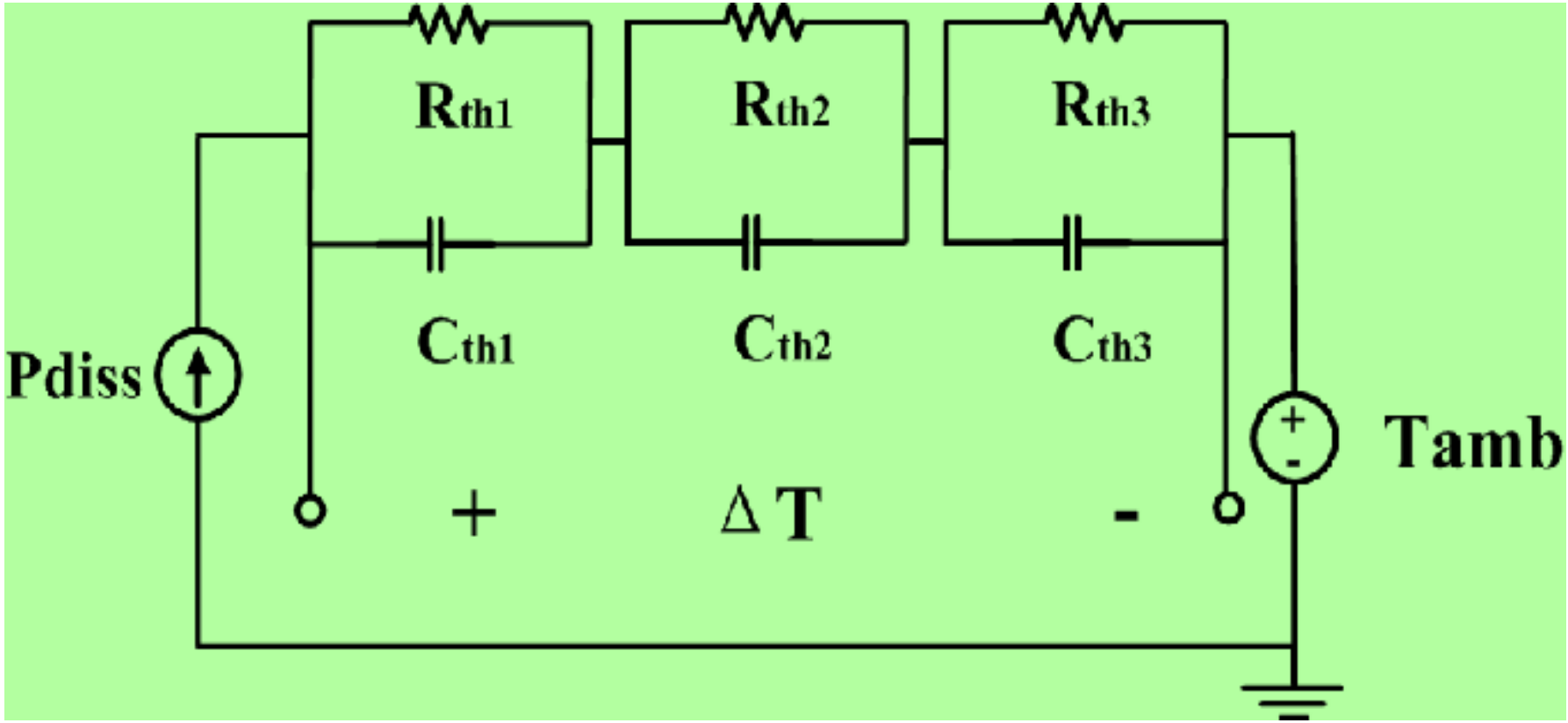
Rate of heat transfer ↔ *Electric current*

Thermal resistance ↔ *Electrical resistance*

Temperature difference ↔ *Voltage difference*

Thermal-electrical analogy: thermal network

Thermal resistance is a heat property of a material that resists a heat flow.



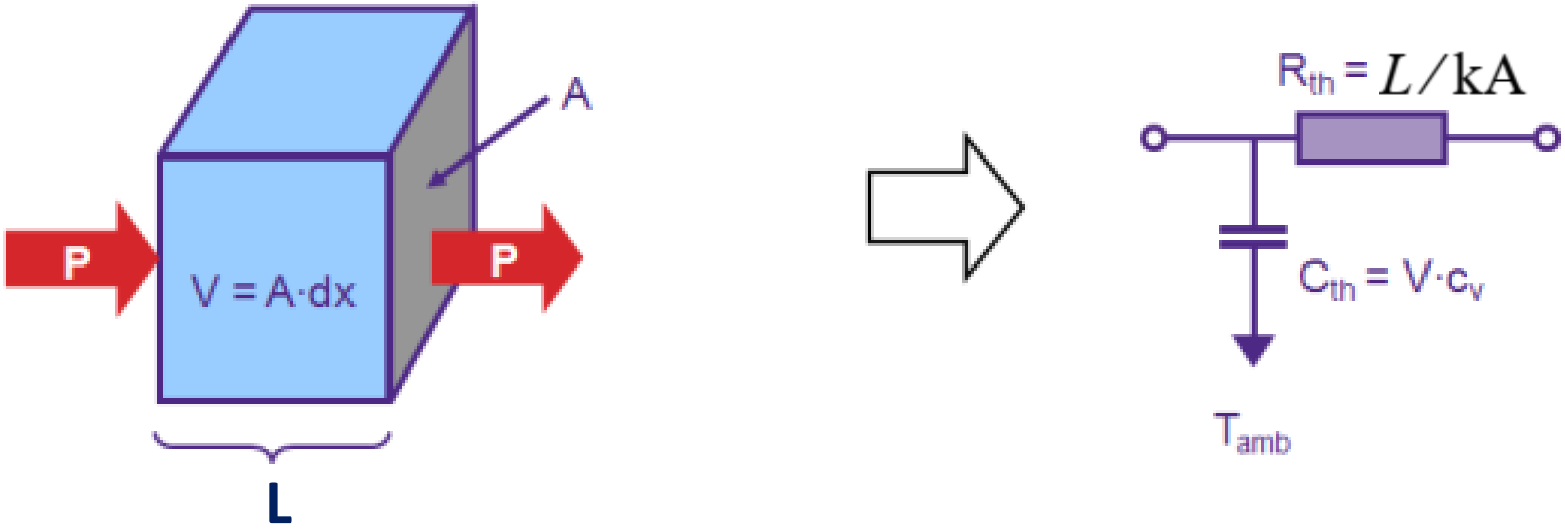
Thermal capacitance is the ability of a body to store thermal energy.

Heat conduction in a piece of solid material.

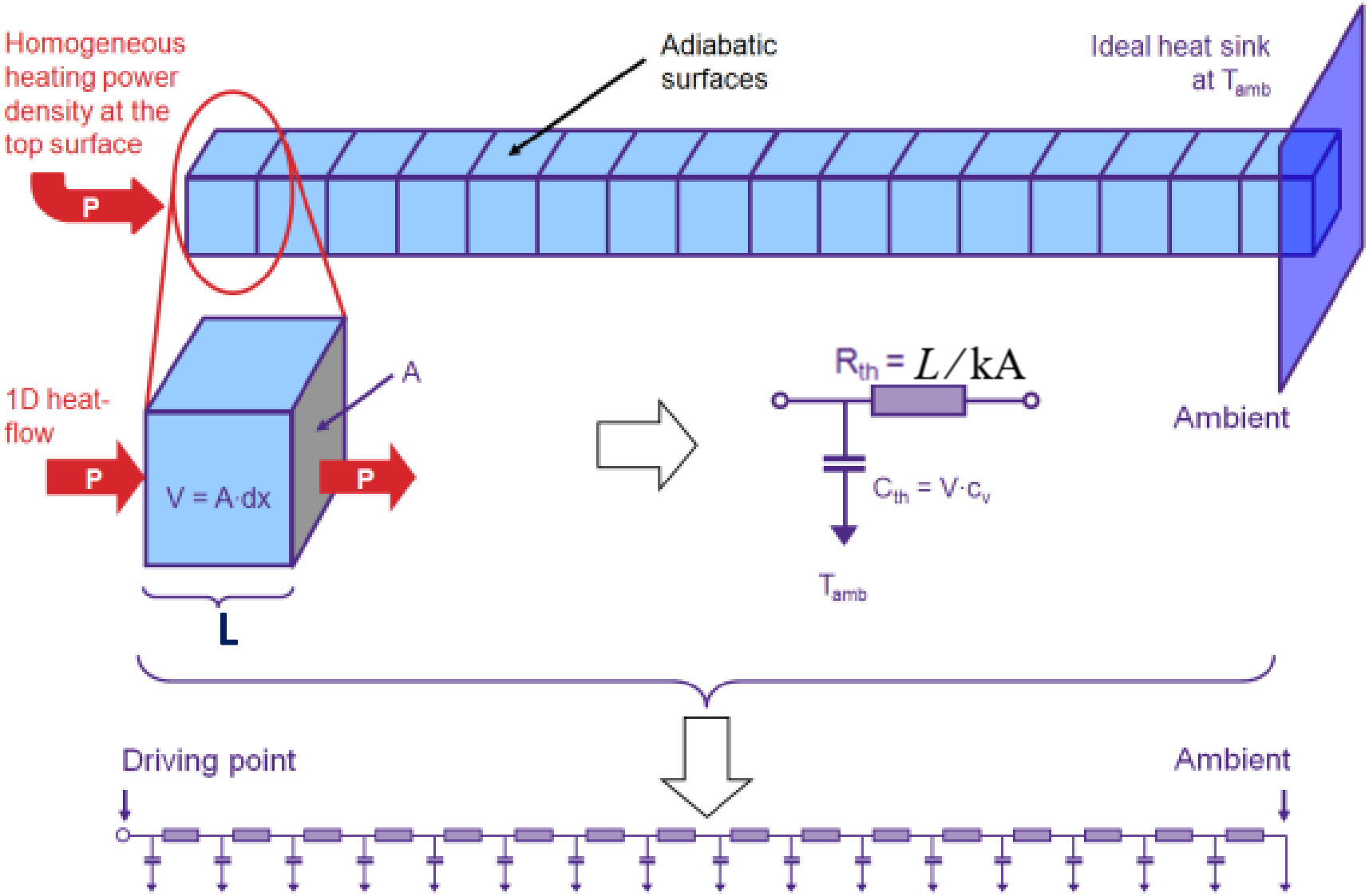
- Lumped model, differential equation replaced by algebraic equation
- Length L, cross-sectional area A, thermal conductivity k.

$$q = \frac{\Delta T}{L/\mathrm{kA}}$$

- Concept of thermal resistance and thermal capacitance:



Thermal network model of a homogeneous rod



Thermal time-constant, unit-step response

- For a homogeneous rod with a length of ***L*** and cross-sectional are of ***A*** the total thermal resistance and thermal capacitance are

$$R_{th} = \frac{1}{k}\frac{L}{A} \qquad C_{th} = c_v LA$$

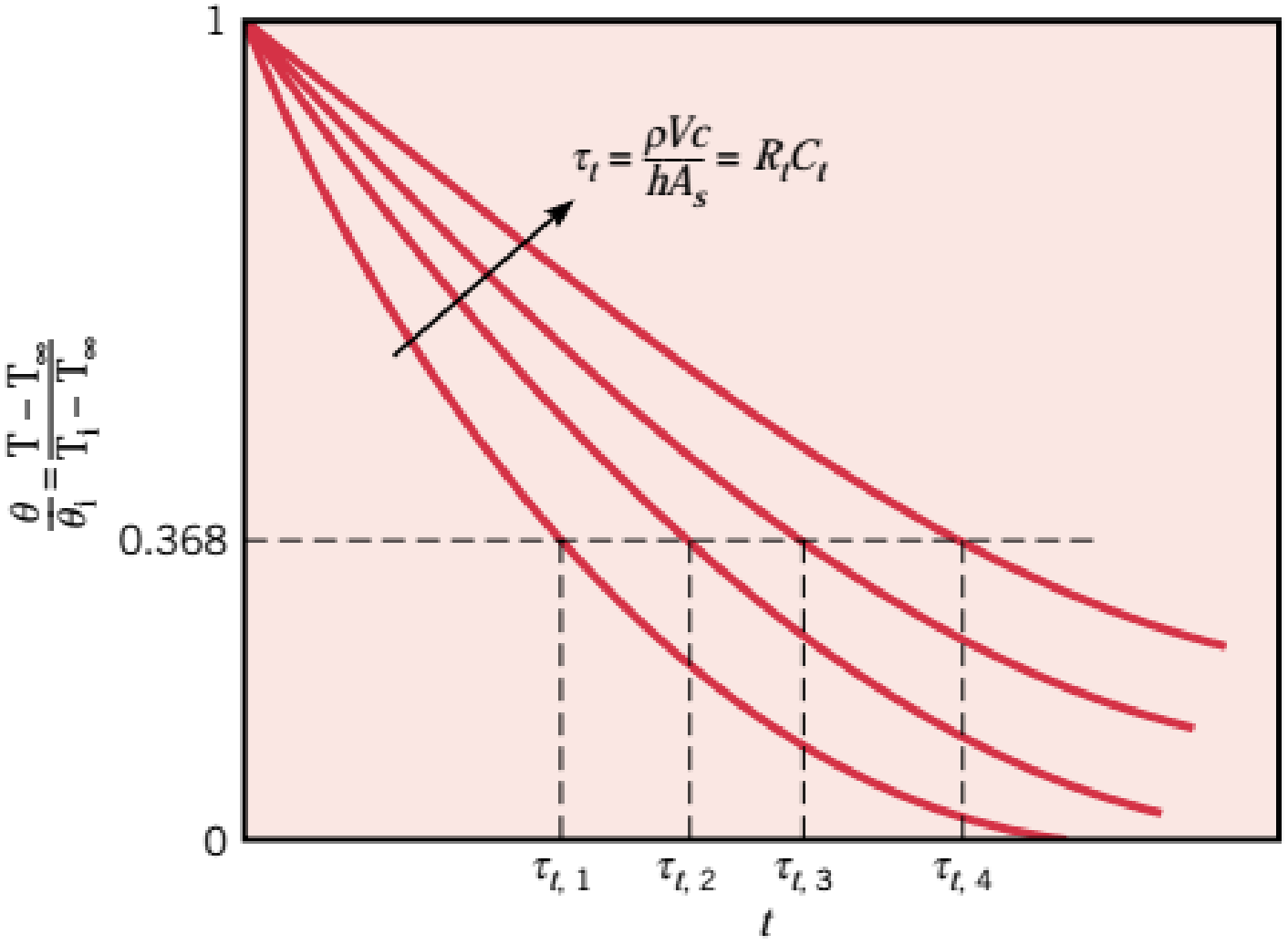
- The thermal time-constant is the product of the thermal resistance and the thermal capacitance (approximate model):

$$\tau = R_{th}C_{th} = \frac{c_v}{k}L^2$$

- The temperature response to a dissipation step with a height of ***P*** can be approximated as

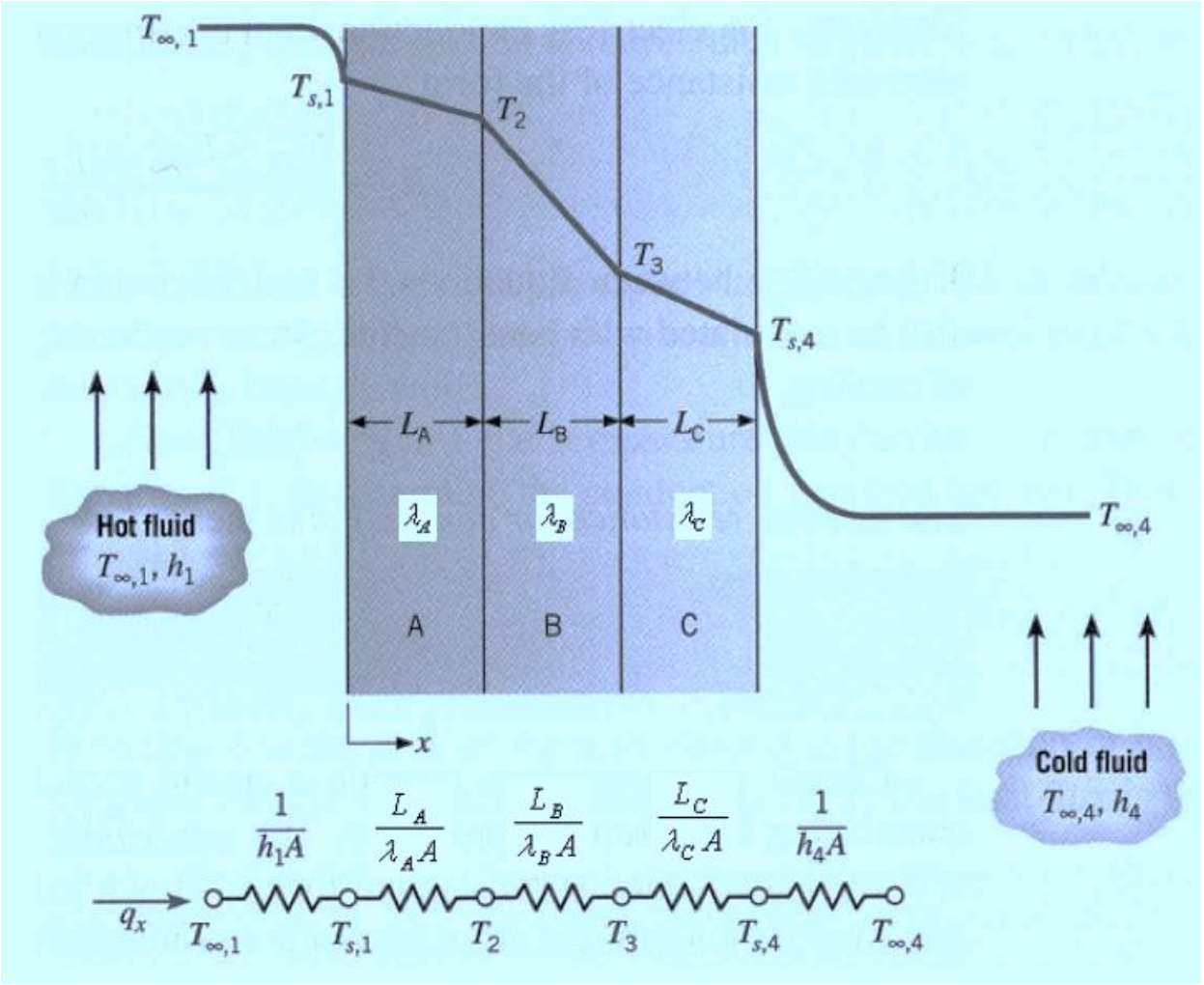
$$T(t) = PR_{th}\exp(1 - t/\tau)$$

Thermal Time Constant



Series and parallel thermal networks

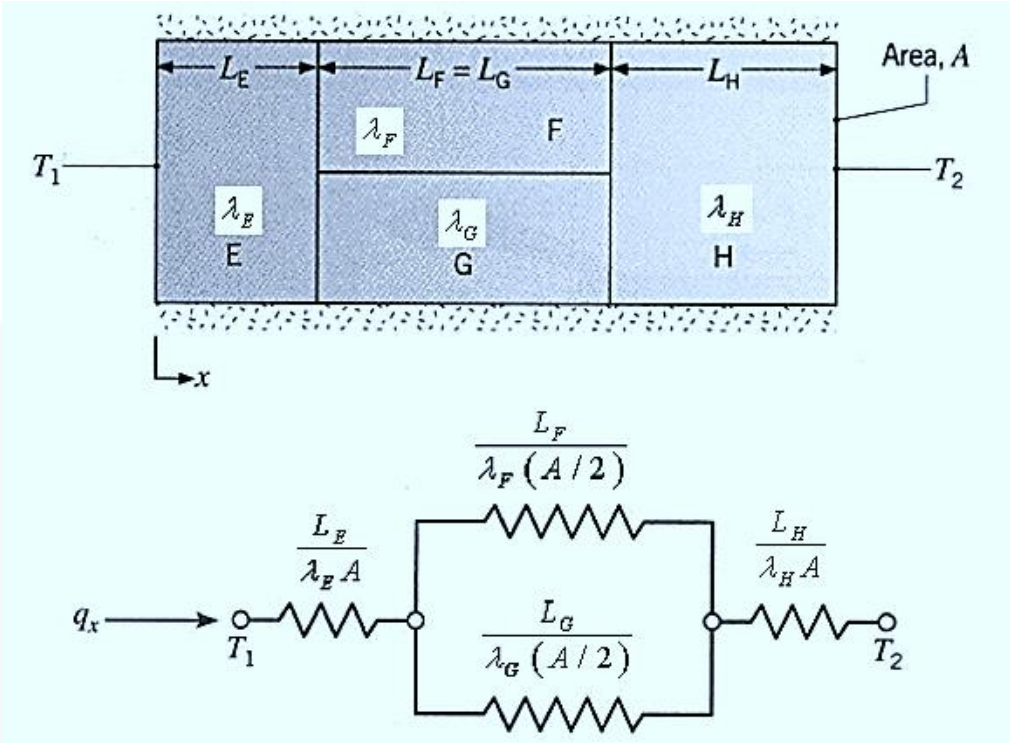
- Series networks:



$$R_{eq} = \frac{T_{\infty,1} - T_{\infty,4}}{q_x} = \frac{1}{A}\left(\frac{1}{h_1} + \frac{L_A}{\lambda_A} + \frac{L_B}{\lambda_B} + \frac{L_C}{\lambda_C} + \frac{1}{h_2}\right)$$

Series and parallel thermal networks

- Parallel networks:



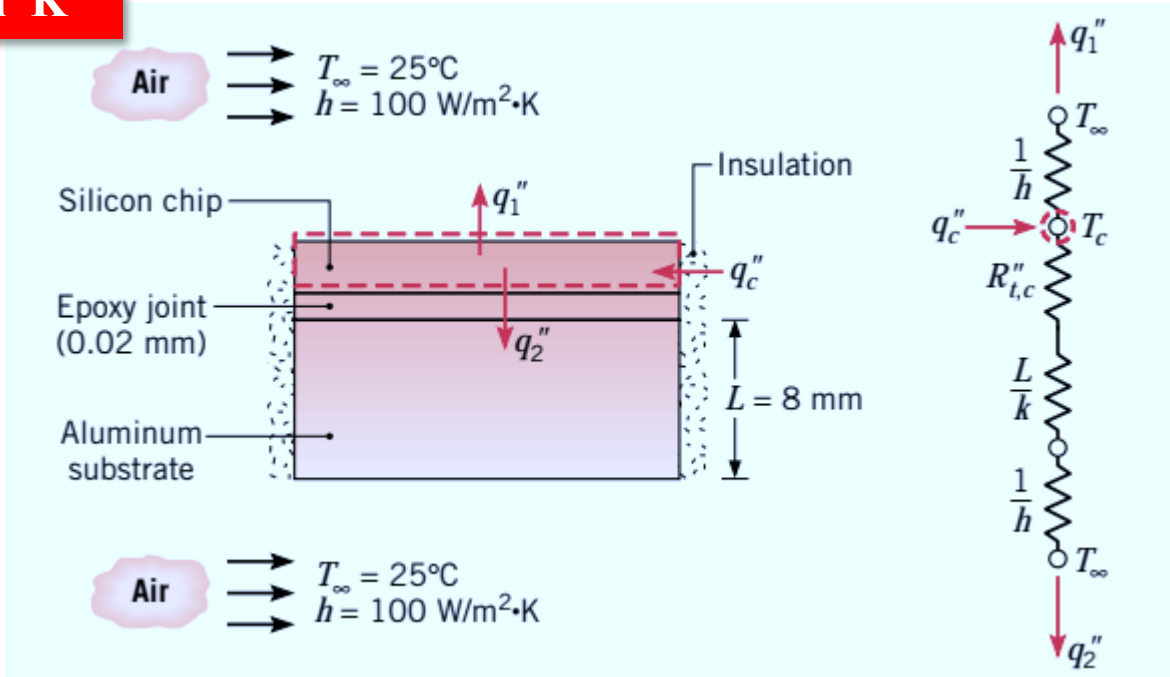
- **Note that this Req will be less than either individual component.**
- **Note that this circuit model is valid only when heat flow is assumed approximately 1-D (if significant heat flow occurred vertically between materials F and G, the resistors-in-parallel model would be invalidated).**

$$R_{eq}^{-1} = \left[\frac{L_F}{\lambda_F (A/2)}\right]^{-1} + \left[\frac{L_G}{\lambda_G (A/2)}\right]^{-1}$$

EXAMPLE

A thin silicon chip and an 8-mm-thick aluminum substrate are separated by a 0.02-mm-thick epoxy joint. The chip and substrate are each 10 mm on a side, and their exposed surfaces are cooled by air, which is at a temperature of 25°C and provides a convection coefficient of 100 $W/m^2 \cdot K$. If the chip dissipates 10^4 W/m^2 under normal conditions, will it operate below a maximum allowable temperature of 85°C?

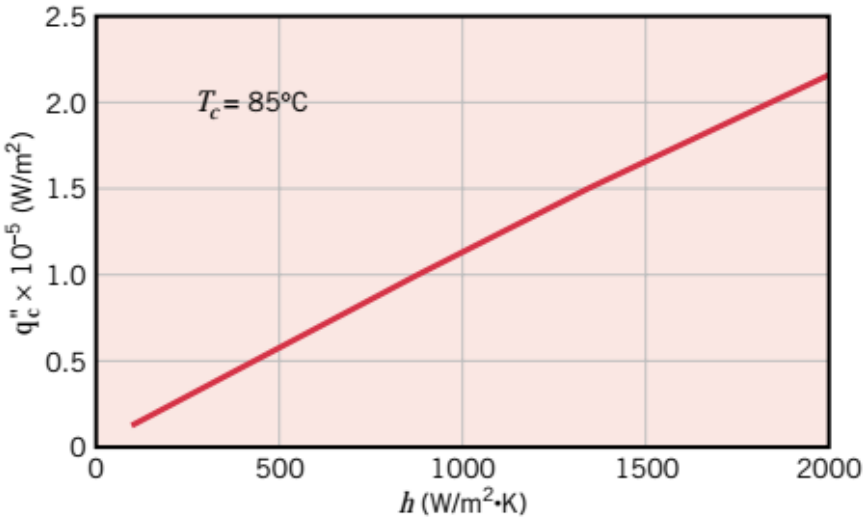
K(AL)= 239 W/m K



Silicon chip/aluminum with 0.02-mm epoxy Rtc= 0.2–0.9 [m^2.K/W]

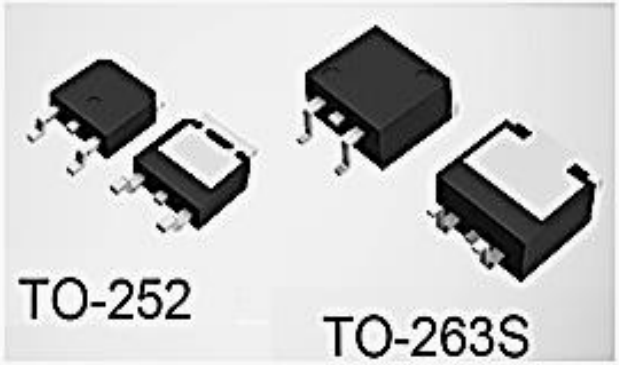
Comments:

1. The joint and substrate thermal resistances are much less than the convection resistance. The joint resistance would have to increase to the unrealistically large value of 50×10^{-4} m$^2 \cdot$ K/W, before the maximum allowable chip temperature would be exceeded.
2. The allowable power dissipation may be increased by increasing the convection coefficients, either by increasing the air velocity and/or by replacing the air with a more effective heat transfer fluid. Exploring this option for $100 \leq h \leq 2000$ W/m$^2 \cdot$ K with $T_c = 85°C$, the following results are obtained.



As $h \to \infty$, $q''_2 \to 0$ and virtually all of the chip power is transferred directly to the fluid stream.

Thermal Resistance in Packaging Design



T_A: Ambient (atmosphere) temperature

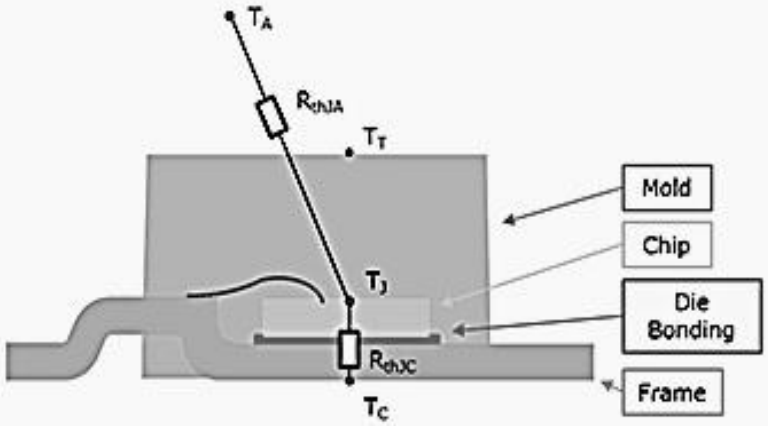
T_J: Junction temperature

T_C: Package back-surface temperature

T_T: Package marking-surface temperature

R_{thJA} (θ_{JA}): Thermal resistance between junction and ambient (atmosphere)

R_{thJC} (θ_{JC}): Thermal resistance between junction and package back surface



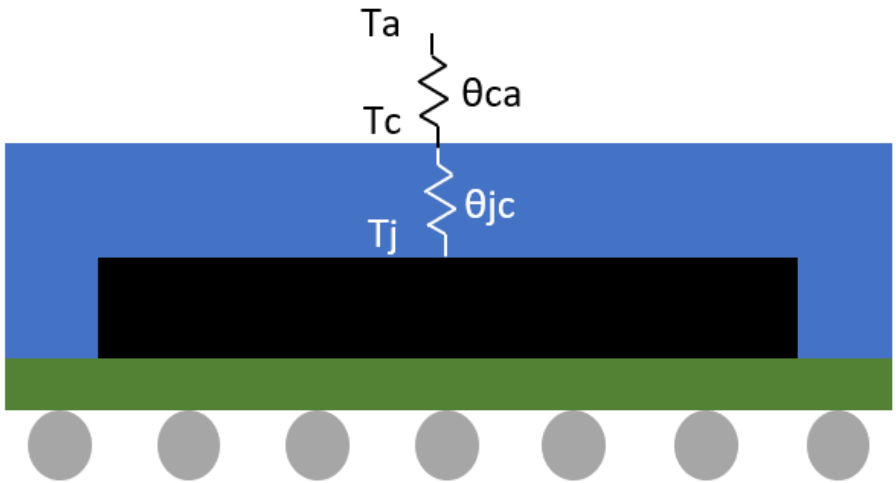
The thermal performance of IC packages is typically measured using the junction-to-ambient and junction-to-case thermal resistance values. These parameters are defined by the following relations:

$$\theta_{jC} = \frac{Tj - Tc}{P}$$

$$\theta_{ca} = \frac{Tc - Ta}{P}$$

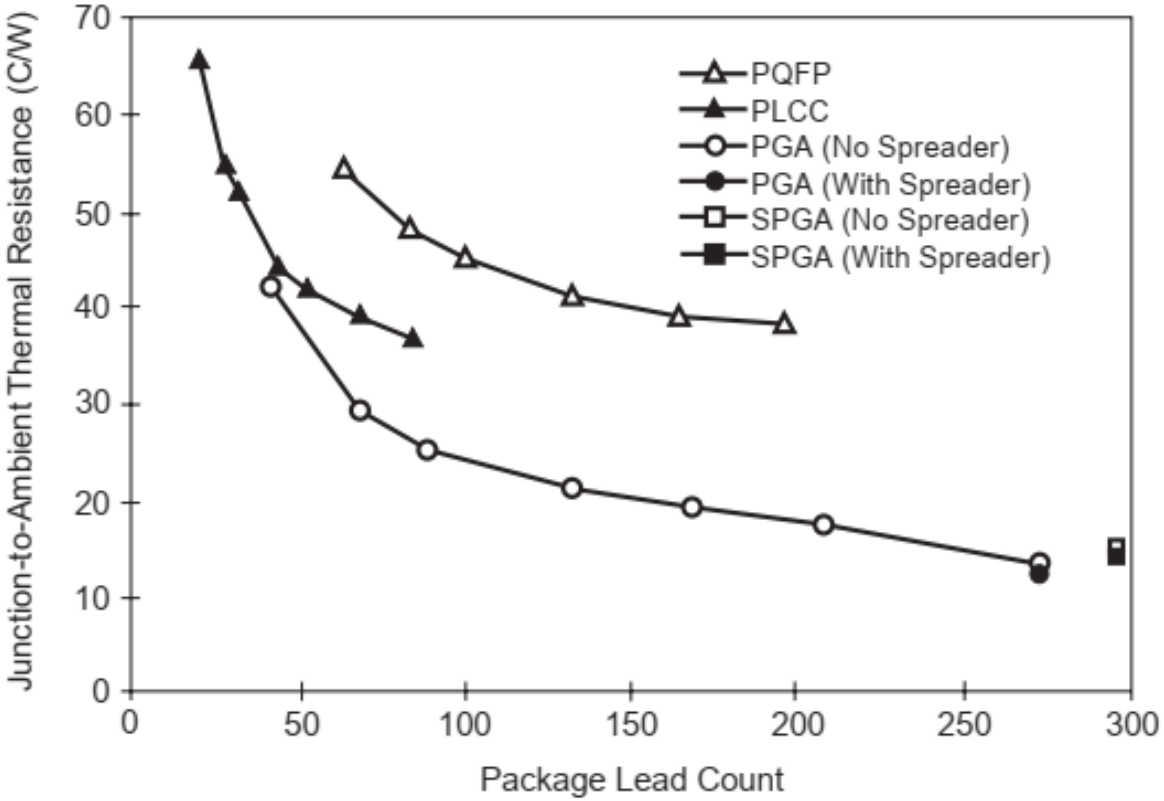
$$\theta_{ja} = \theta_{jc} + \theta_{ca}$$

Packaging materials
Package geometry
Ambient conditions



The thermal resistance of a package is not a constant.

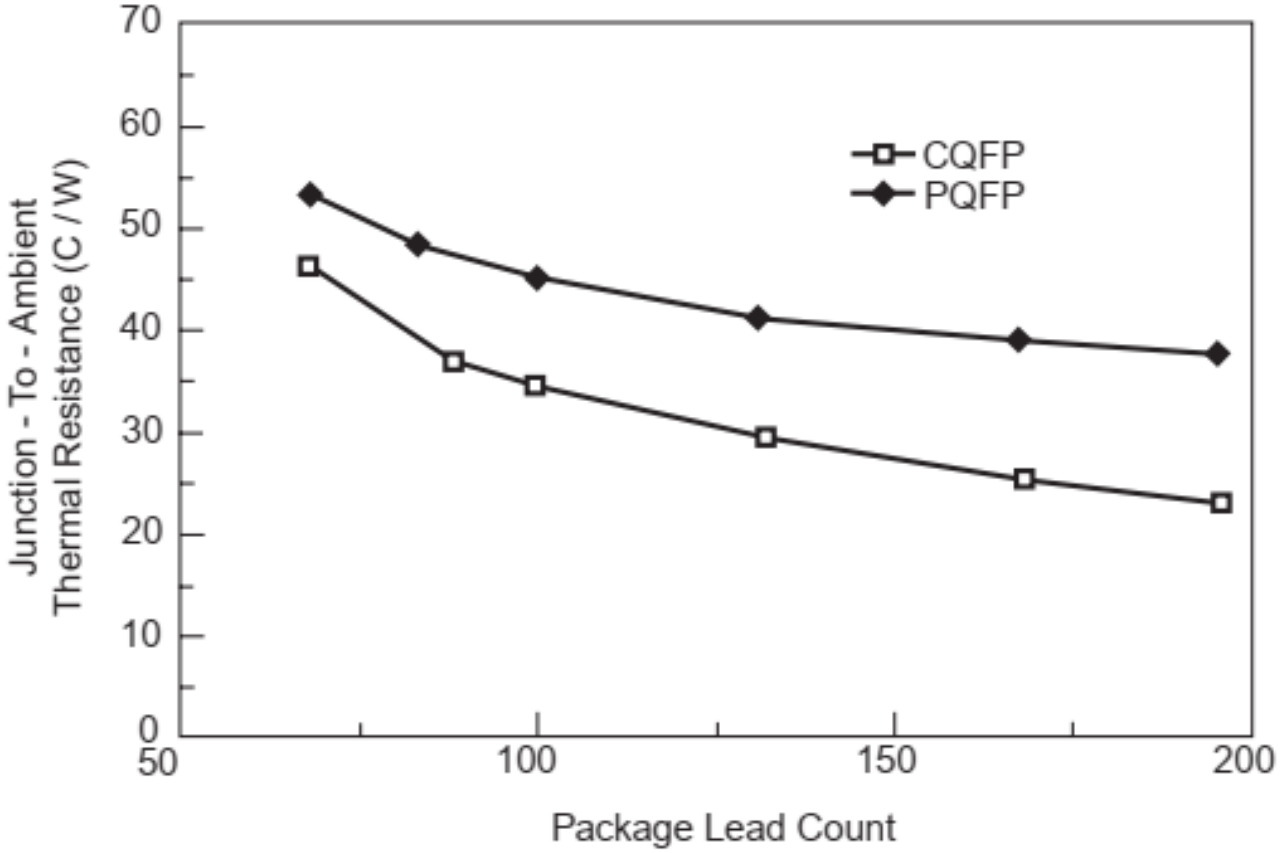
1. Package Size



Effect of Package Size on Thermal Resistance of PLCC, PQFP, and PGA Packages

The thermal resistance of a package is not a constant.

2. Packaging Material Thermal Conductivity.



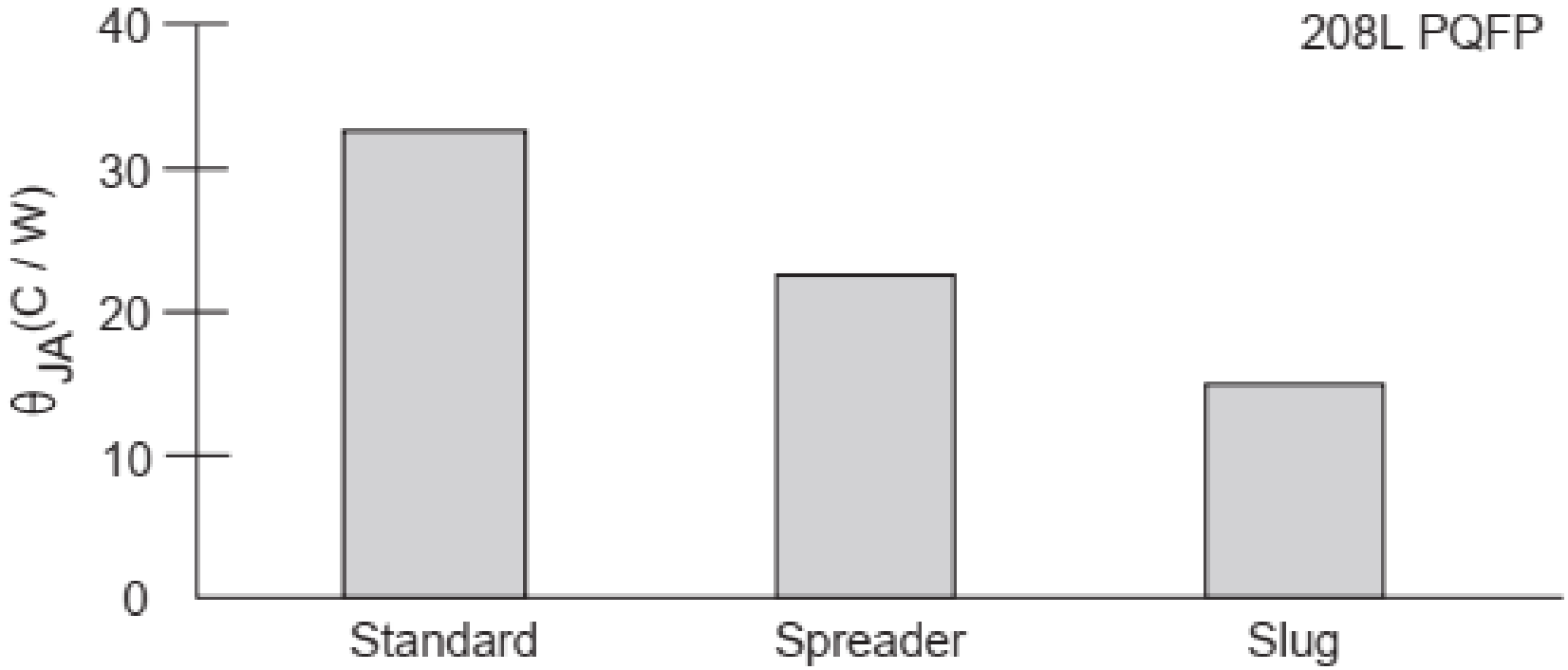
Effect of Packaging Material on Thermal Resistance

The thermal resistance of a package is not a constant.

3. Heat Spreader And Heat Slug.

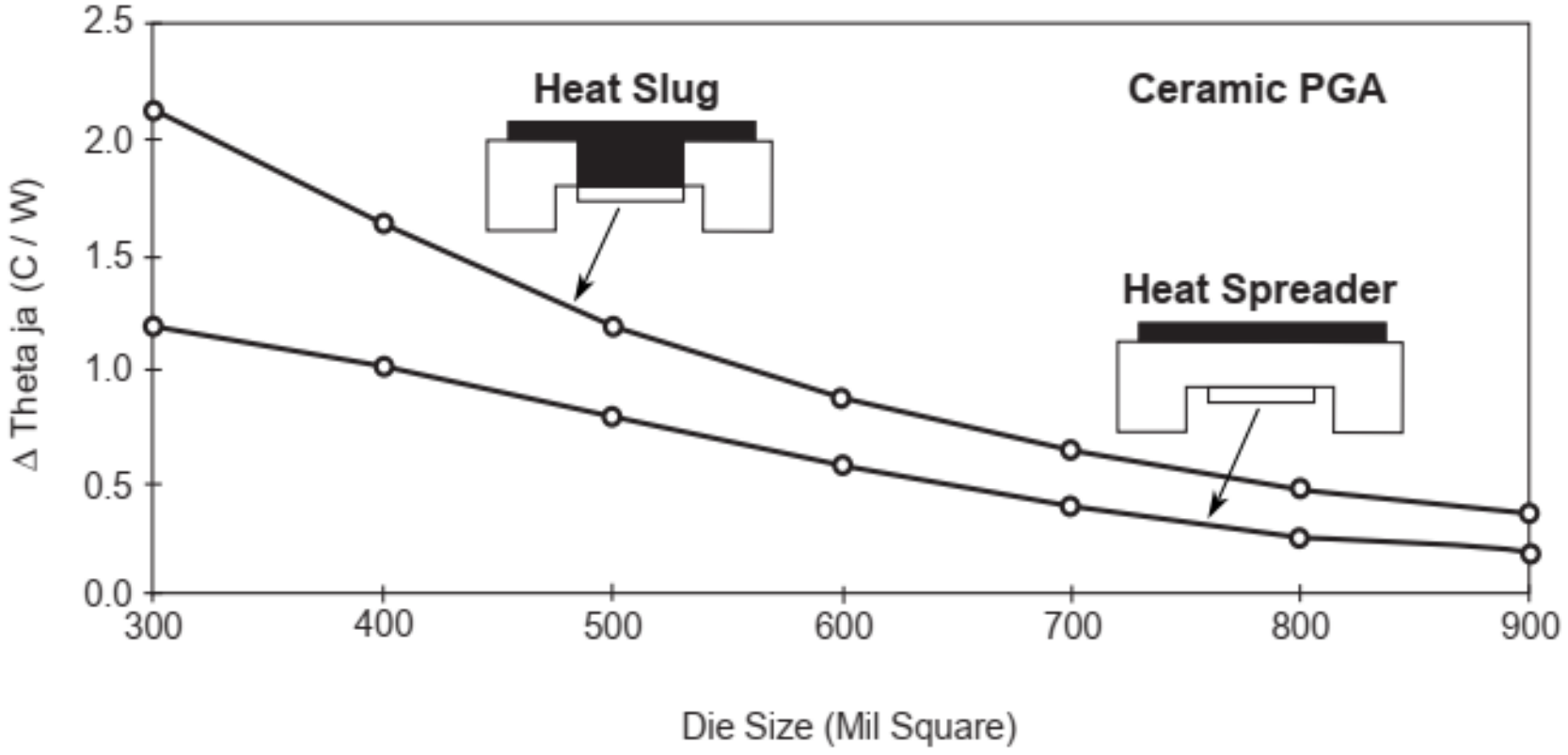
- Heat spreaders and heat slugs are commonly used to improve the heat spreading effect which results in lower package internal thermal resistance.
- For lead frame type packages (such as PQFP and SQFP) the heat spreader plate is typically made from Copper or Aluminum and is attached to the bottom surface of the lead frame.
- For CPGA type packages, the heat spreader is typically made from Copper or Copper-Tungsten alloy and is attached to the top surface of the ceramic packages.
- For both types of packages, the heat slug is a metal block which on the one side is attached to the die and on the other side is exposed to the outside environment.
- The effect of heat spreaders and heat slugs on thermal performance is more significant for smaller die sizes.

The difference of thermal resistance for different PQFP package types



Heat Spreader and Heat Slug Compared to Standard Package of PQFP

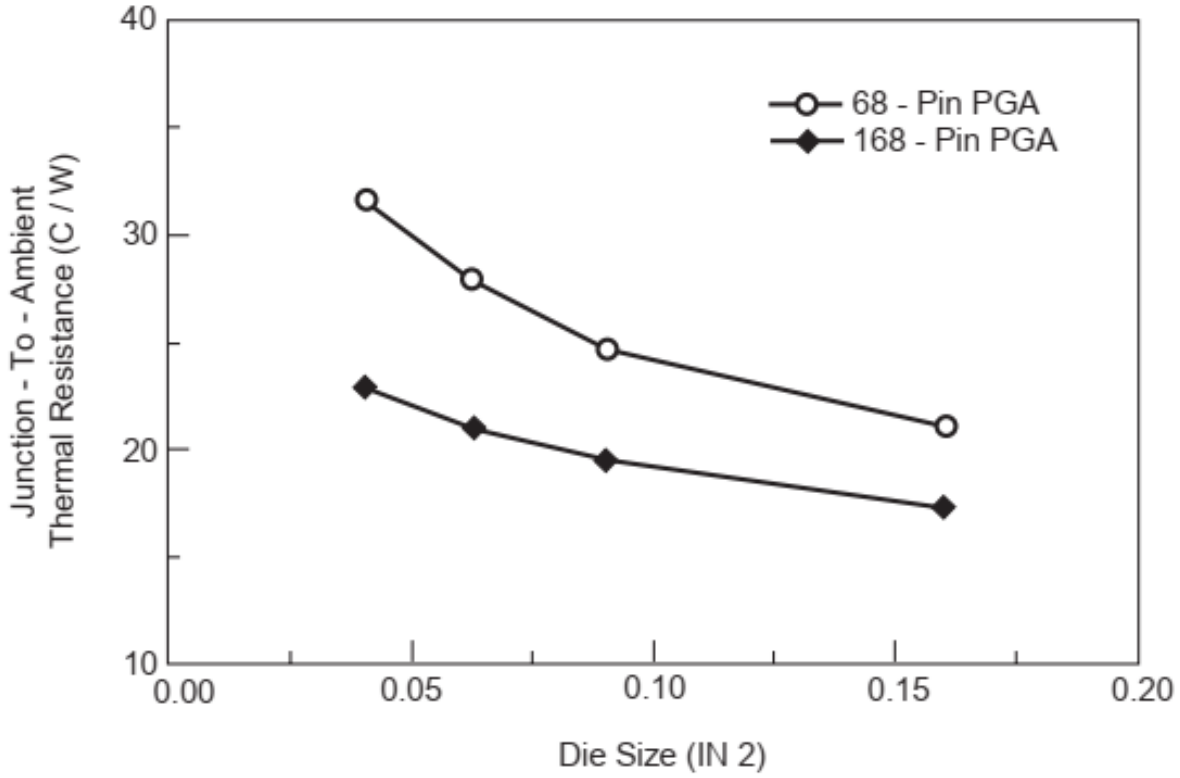
The reduction of θja for CPGA packages by using heat spreader and heat slug.



Effect of Heat Spreader and Heat Slug on Thermal Performance

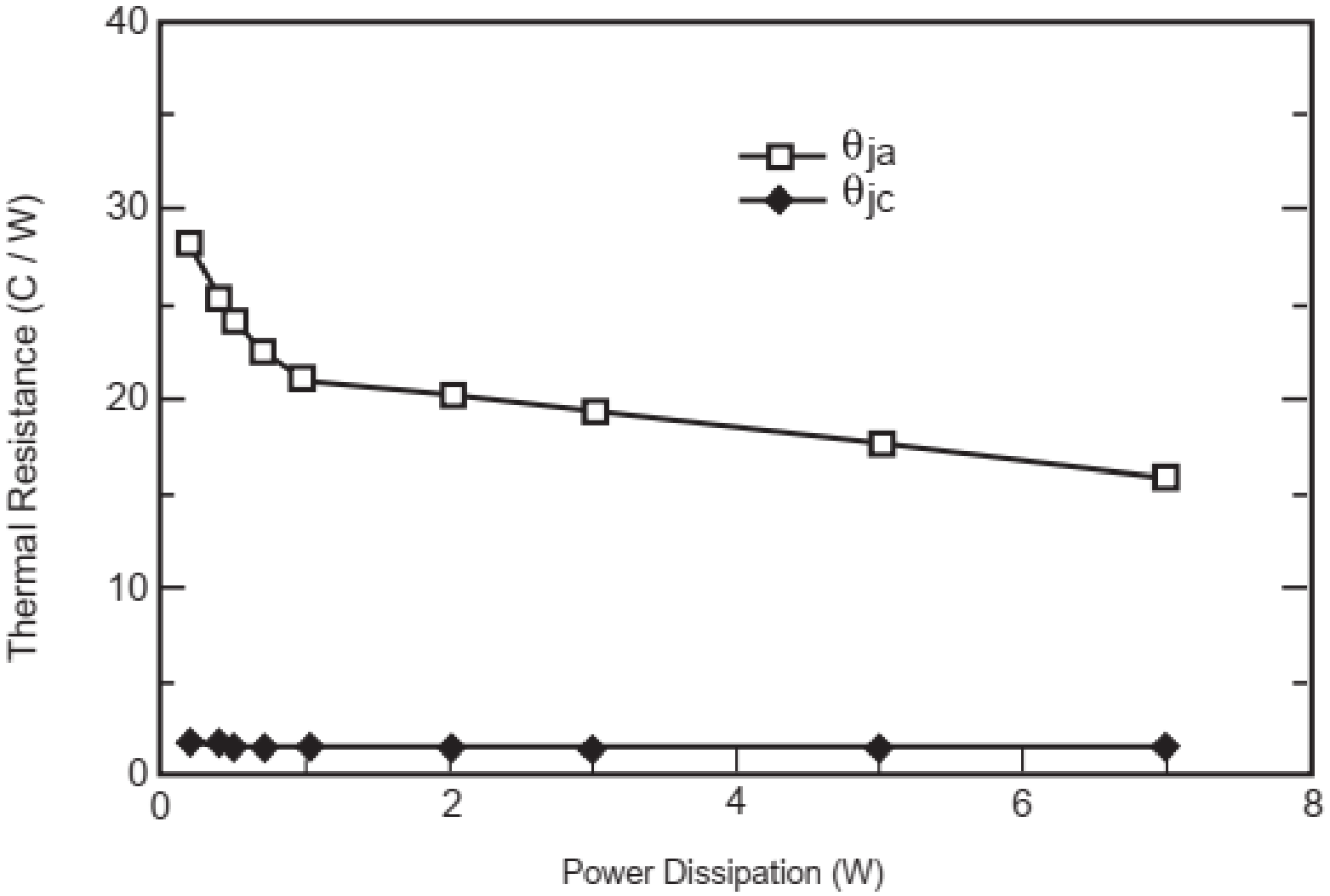
4. Die Size

- Thermal resistance decreases as the die sizes increases.
- Increase in die size results in lower power density and larger effective heat transfer area.
- The changes in thermal resistance are sharper at smaller die sizes, and as the die size approaches packages size, they become less significant.



Effect of Die Size on Package Thermal Resistance

5. Device Power Dissipation.



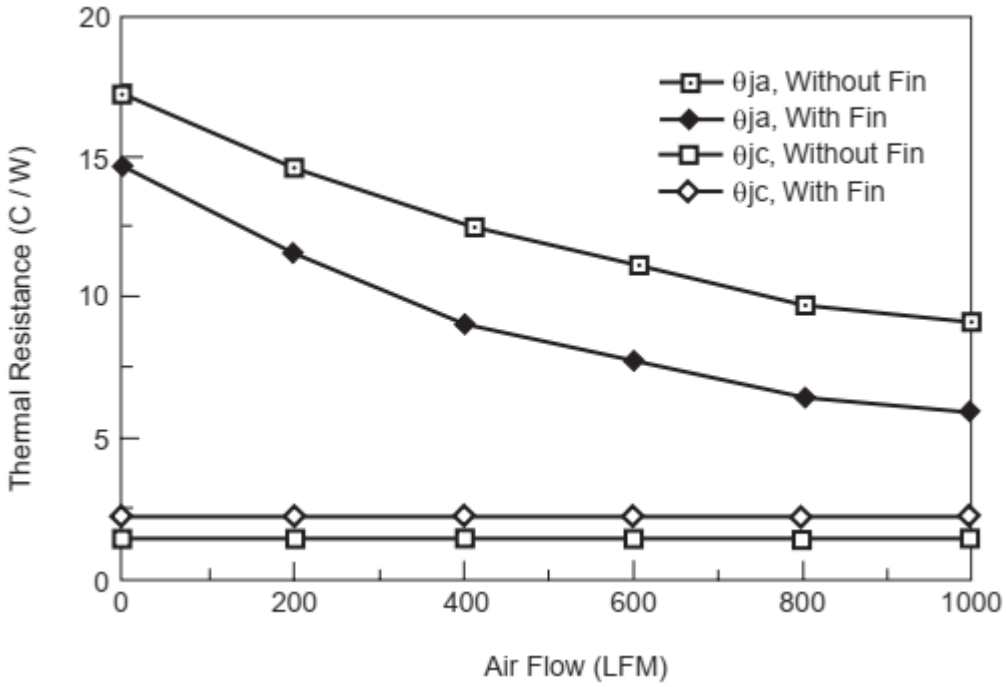
Effect of Power Dissipation on Thermal Resistance

6. Air Flow Rate

In forced convection, case-to-ambient thermal resistance is a function of the air flow rate:

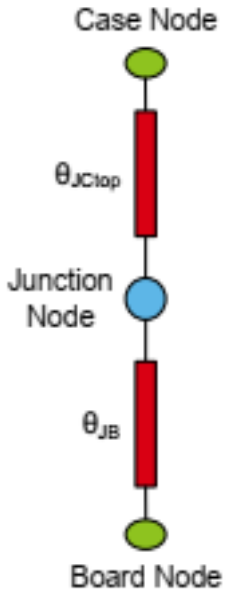
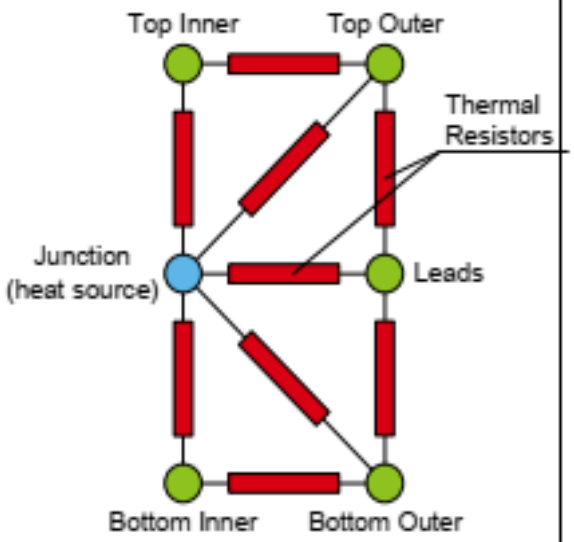
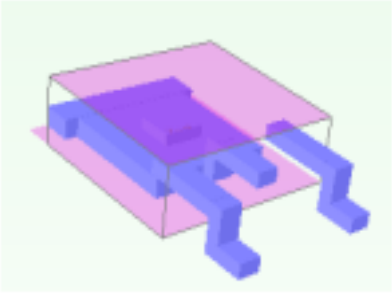
$$\theta_{ca} = K / V^{m}$$

K = Constant depending on air properties as well as package geometry.
V = Air velocity (m/s)
m = 1/2 and 4/5 for laminar and turbulent flow respectively.



Effect of Air Flow Rate on Thermal Resistance of 168-Lead PGA Package

Thermal Simulation

Type	Compact thermal model (CTM)		Detailed model
	Two-resistor model	DELPHI model	
Standard	JESD15-3	JESD15-4	N.A.
Shape			
Summary	• Simple model only dividing a package vertically at the junction • Ideal for single function devices such as discrete products	• Model representing a package with a multi-resistor network	• Detailed model including details of dimensions and physical properties of materials
Precision	Good	Better	Best
Shortcomings	• Least precise among the 3 models • Transient analysis not supported	• Transient analysis not supported	• Variation in quality without any standard • Long simulation time • No compatibility between tools

References

- **IC Packages Performance Characteristics: Databook, Ch 4 (intel.com)**
- **Two-Resistor Model for Thermal Simulation [ROHM]**
- ***Fundamentals of Heat and Mass Transfer [*FRANK P. INCROPERA]**

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Department of Electron Devices

Circuit Environment

Lecture 10

Signal Integrity III

Transmission Lines and Reflections

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2021/2022

TRANSMISSION LINES AND UNINTENTIONAL DISCONTINUITIES

Signal sees an impedance change

There will be a reflection

Reflections impact on signal quality

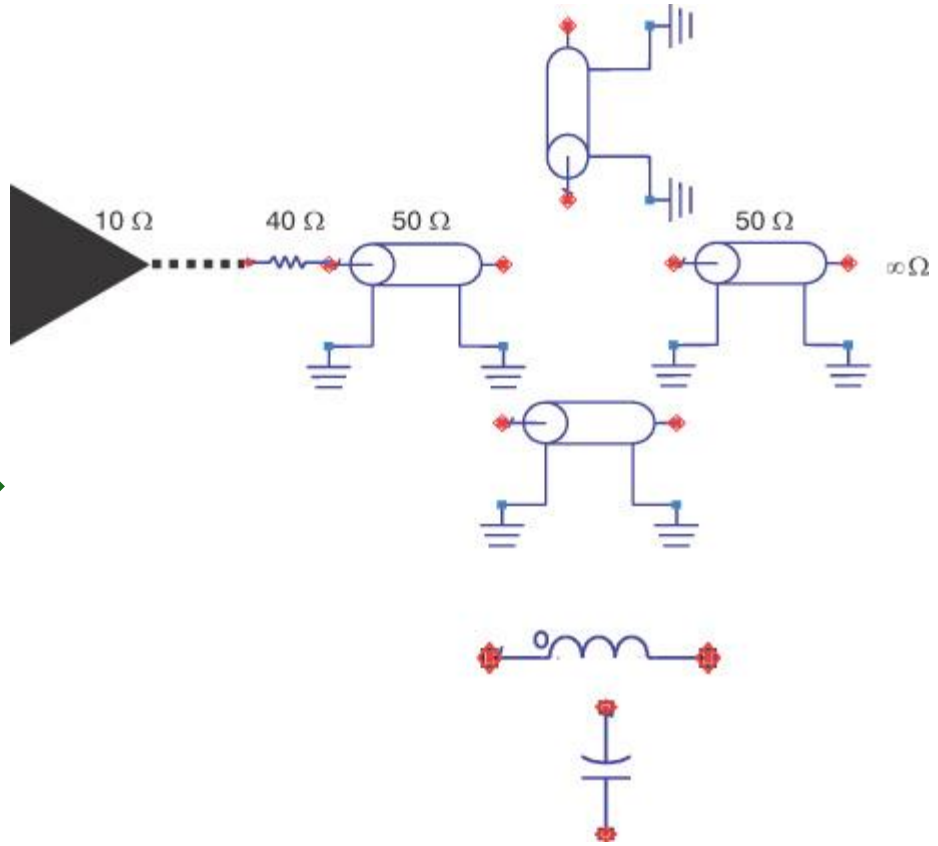
Predicting the impact on the signals

An important part of signal-integrity engineering.

UNINTENTIONAL DISCONTINUITIES

- Even if a circuit board is designed with **controlled impedance interconnects**.
- There is still the opportunity for a signal to see an **impedance discontinuity** from such features as:

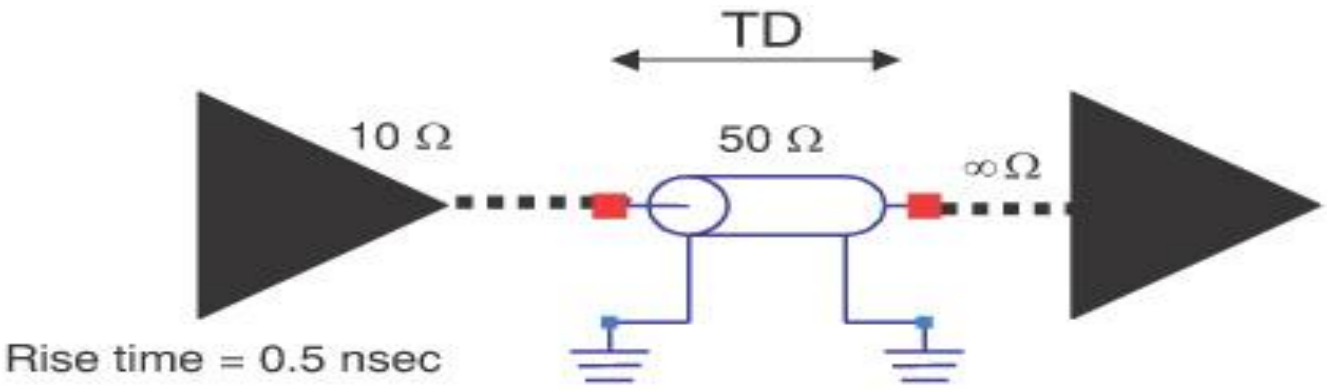
- The ends of the line
- A package lead
- An input-gate capacitance
- A via between signal layers
- A corner
- A stub
- A branch
- A test pad
- A gap in the return path
- A neck down in a via field
- A crossover



WHEN TO TERMINATE

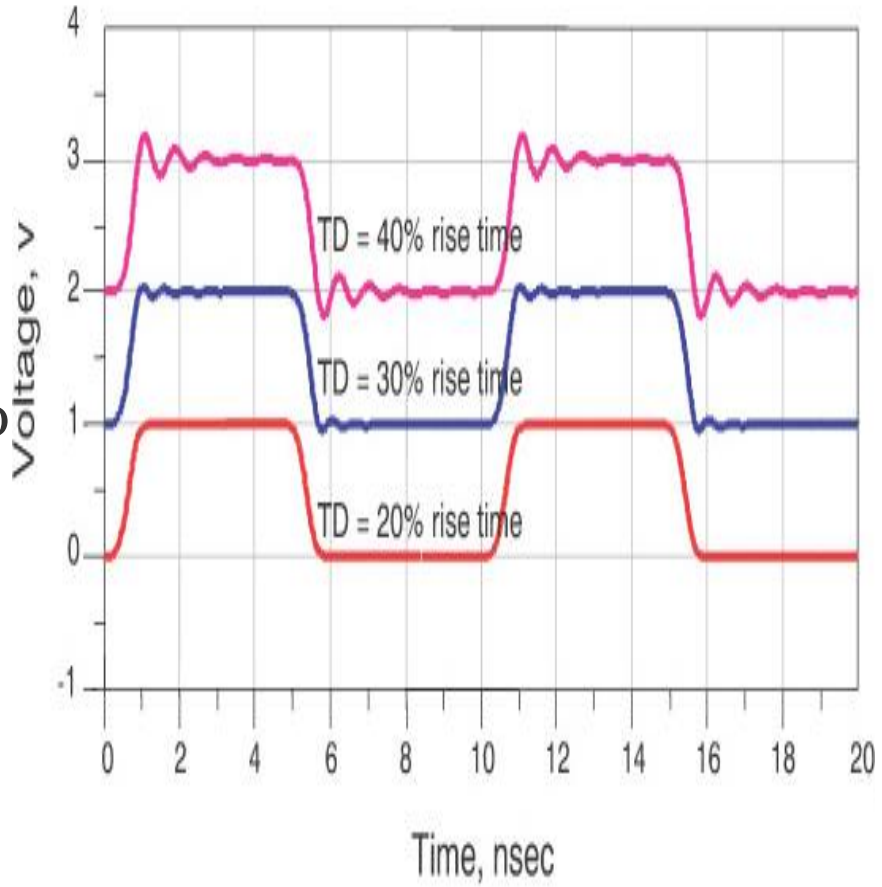
- The simplest transmission-line circuit has
  1. a driver at one end,
  2. a short length of controlled-impedance line,
  3. a receiver at the far end.

- The signal will bounce around between the high impedance open at the far end and the low impedance of the driver at the sending end.
- When the line is long, these multiple bounces will cause signal-quality problems, which classified as a ringing noise.



WHEN TO TERMINATE

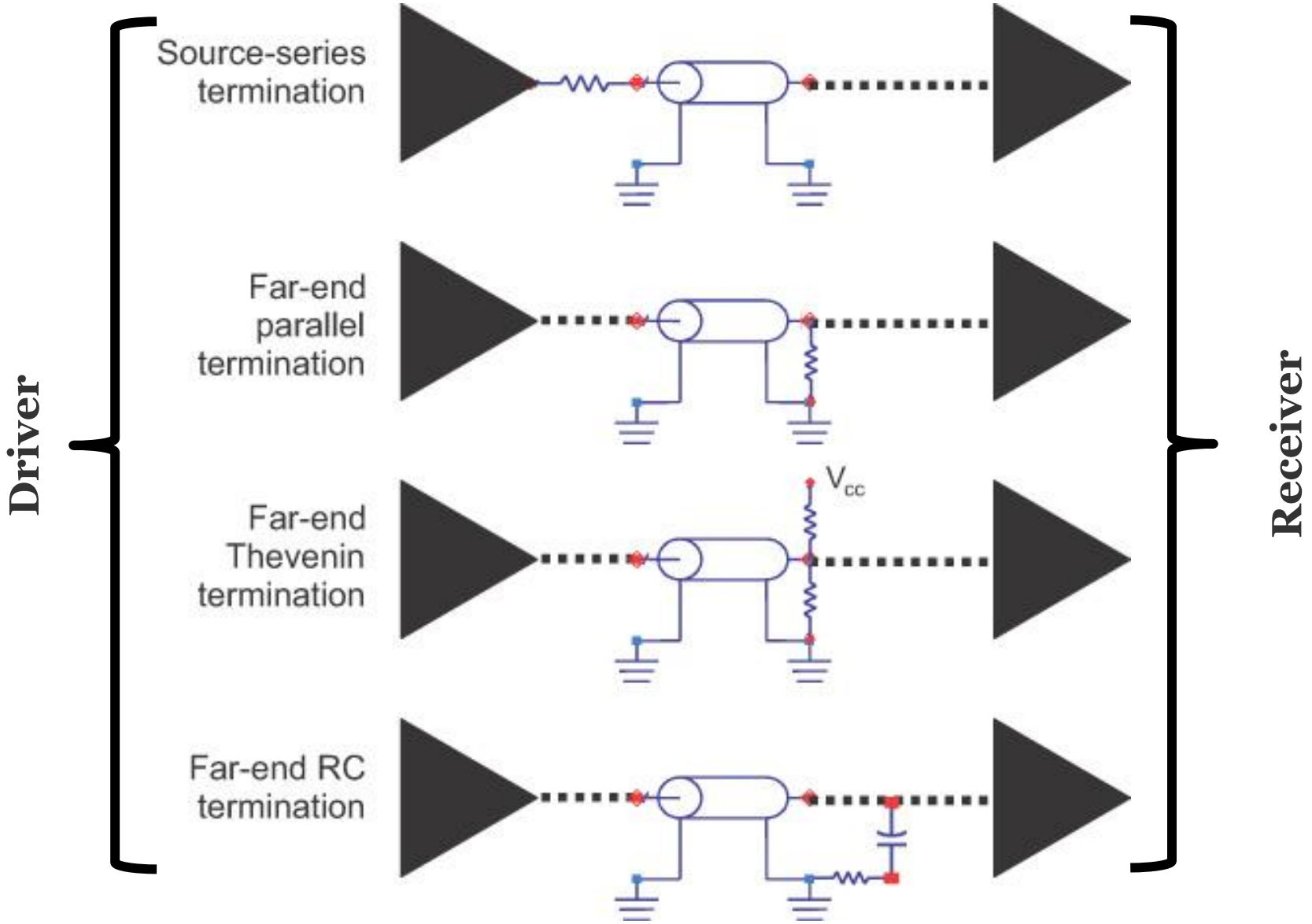
- But if the line is short enough, though the reflections will still happen, but they are smeared out with the rising or falling edge and may not pose a problem.
- The threshold of **TD > 20%** of the rise time as the boundary of when to start worrying about ringing noise due to an unterminated line.
- If the TD of the transmission line is greater than 20% of the rise time, ringing will play a role and must be managed.



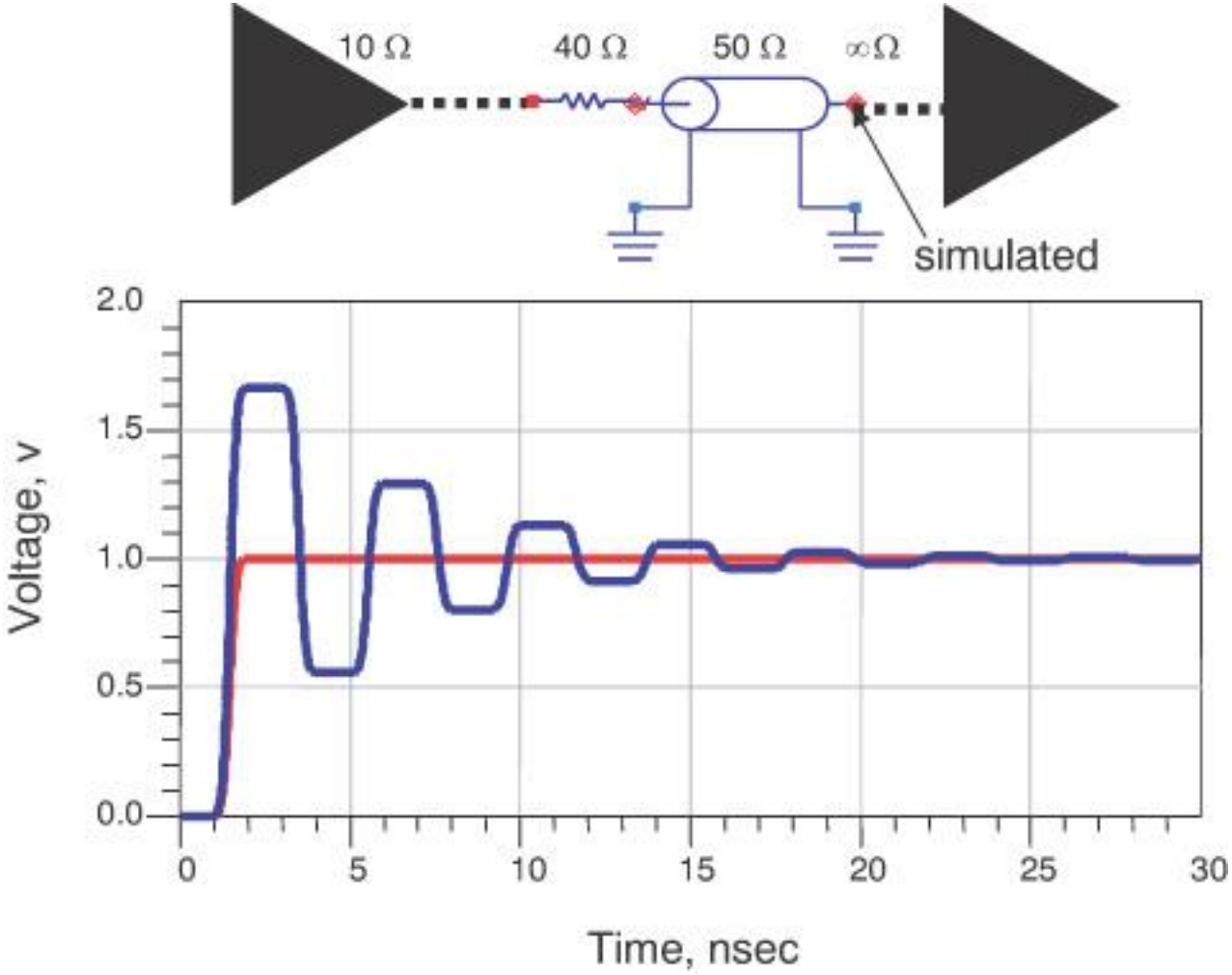
POINT-TO-POINT TOPOLOGY

- The origin of the ringing is the impedance discontinuities .
- If the reflections are eliminated from at least one end, result in minimize the ringing.
- Design the impedance at one or both ends of a transmission line to minimize reflections is called **terminating the line.**
- When **one driver drives one receiver**, we call this a **point-to-point topology.**
- There are four techniques to **terminate a point-to-point** topology.

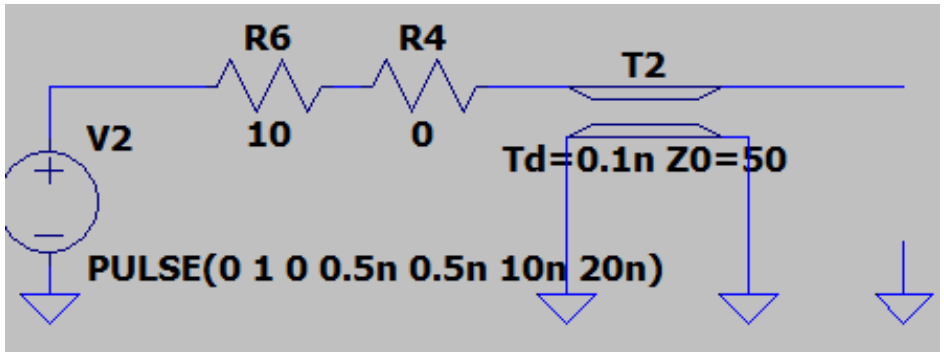
POINT-TO-POINT TOPOLOGY

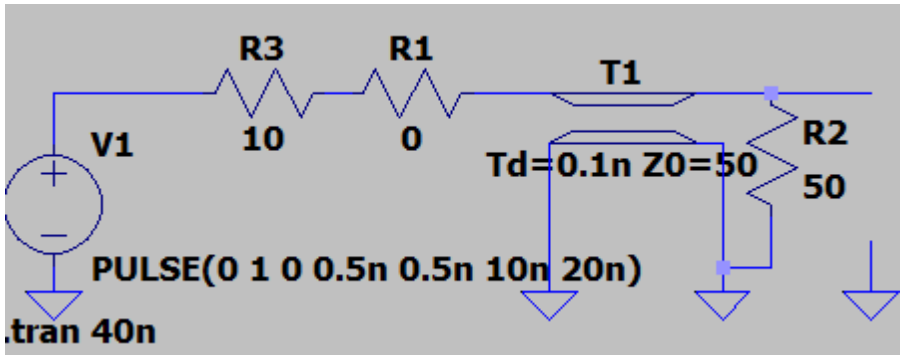


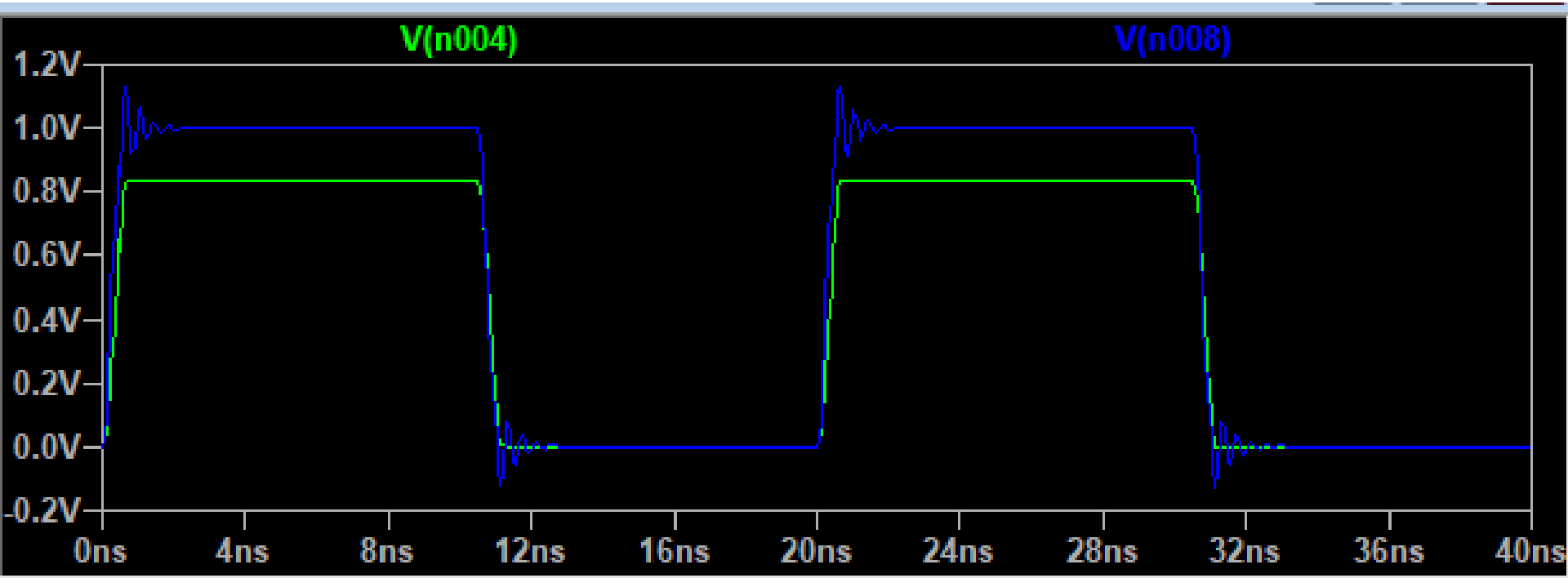
Source-series termination



Parallel Termination





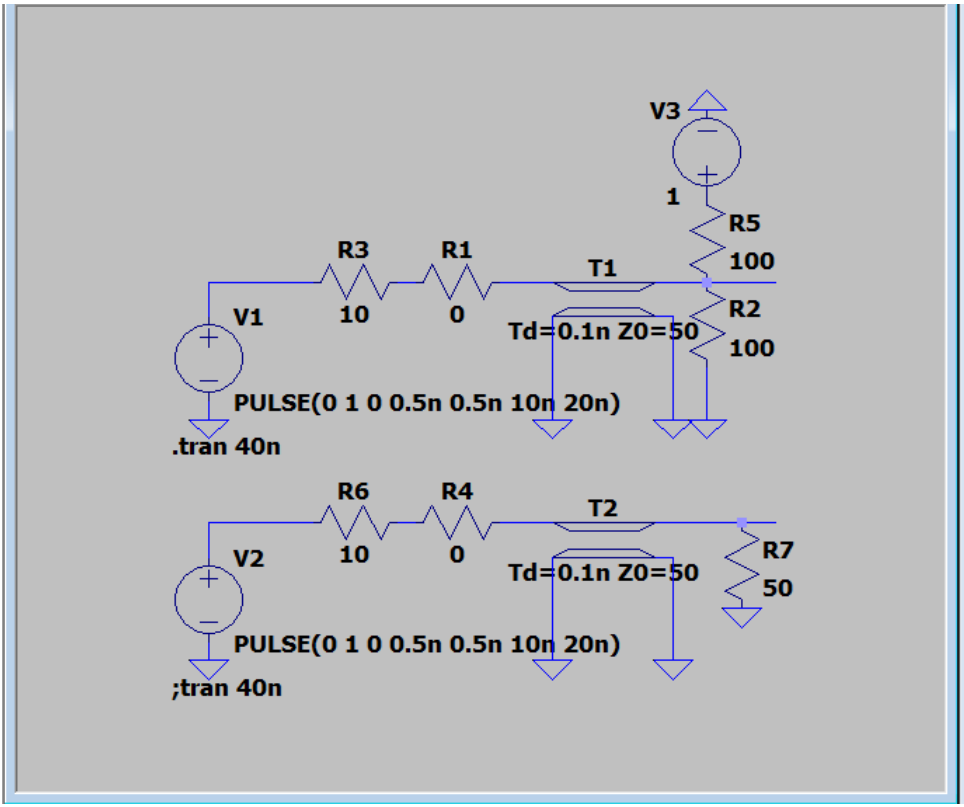


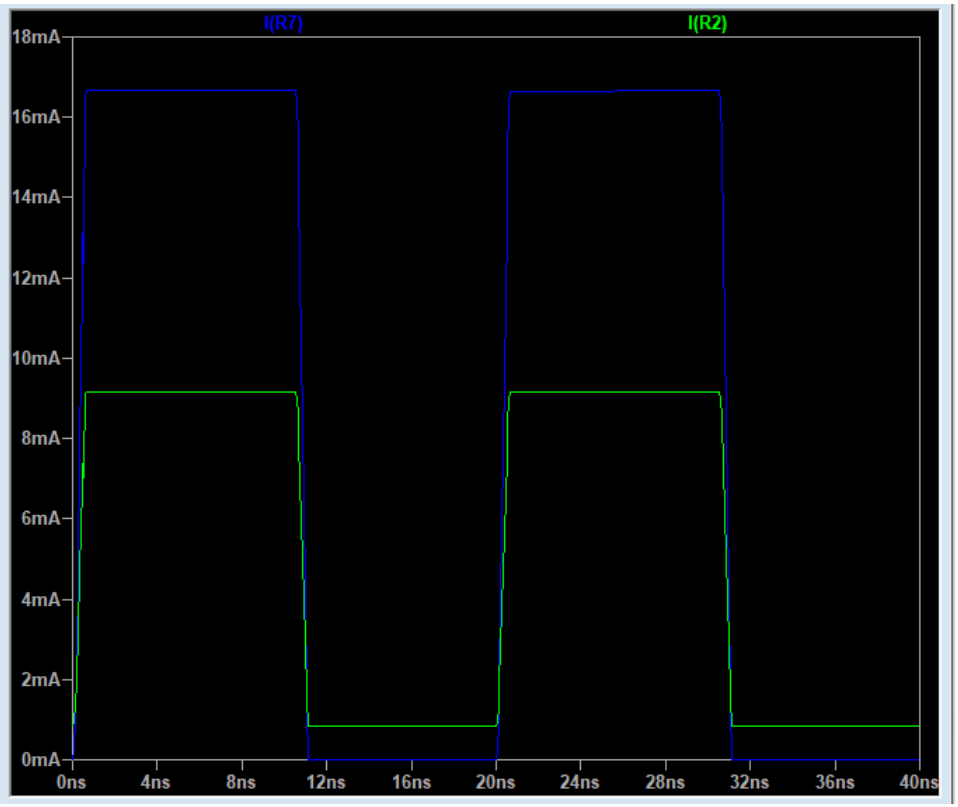
Thevenin termination

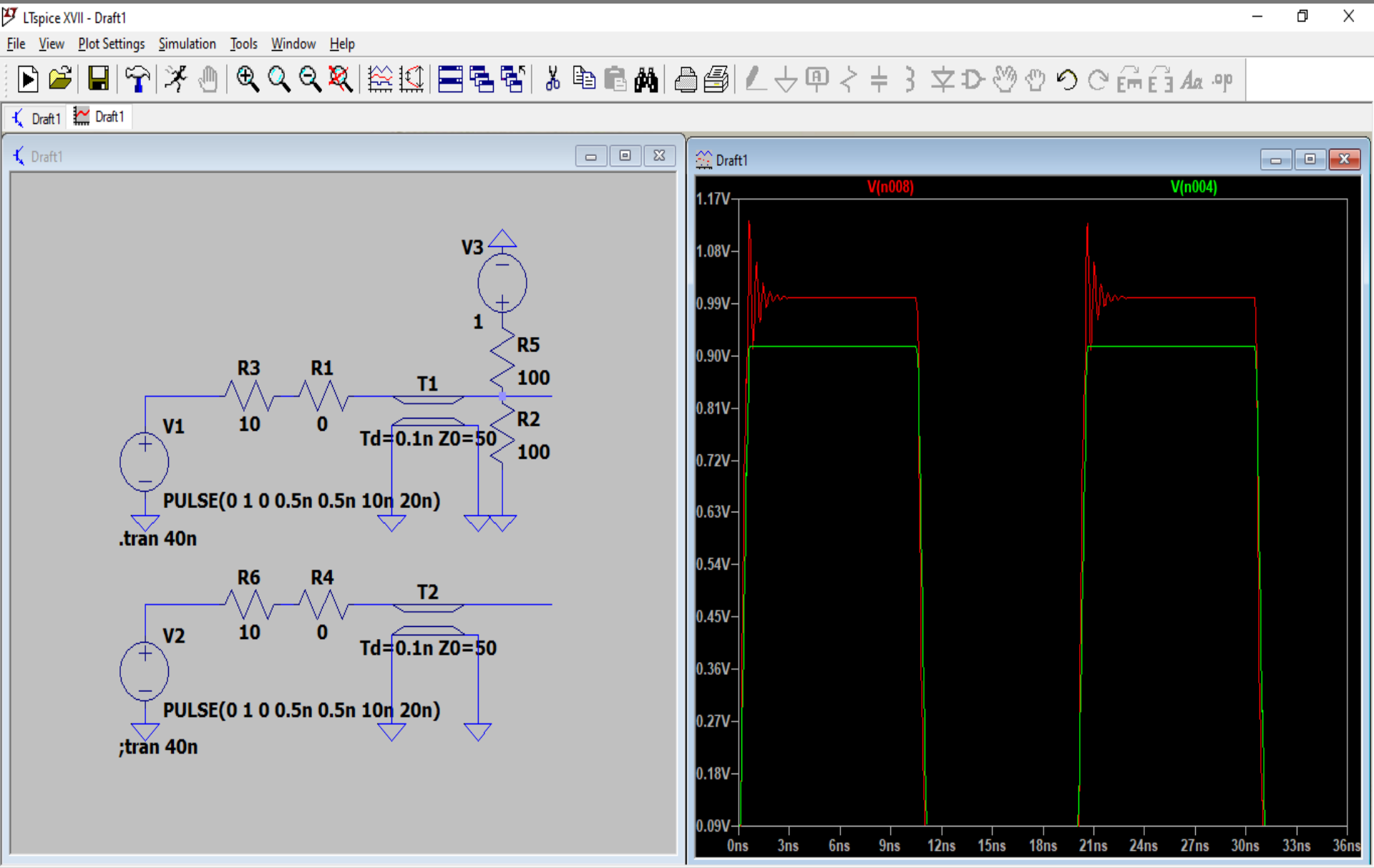
- Thevenin termination is similar to parallel termination, except that both pull−up and pull−down resistors are used.
- Power consumptions are also similar for both of these schemes.
- The difference is that the DC power consumption is a function of duty cycle and resistor ratios.
- If the resistors are matched, DC power consumption is not dependent upon duty cycle.
- One advantage Thevenin termination has over parallel termination is that lines with impedances as low as 50 can be terminated in their characteristic impedances.
- For proper impedance matching, the equivalent Thevenin resistance should be the same as the line characteristic impedance

Thevenin termination

- The






LTspice XVII - Draft1
File View Plot Settings Simulation Tools Window Help
Draft1
Draft1
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V3
1
R5
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R3
R1
T1
R2
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Td=0.1n Z0=50
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R4
T2
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Td=0.1n Z0=50
PULSE(0 1 0 0.5n 0.5n 10n 20n)
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V(n008)
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0.99V
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0.81V
0.72V
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0.54V
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0.36V
0.27V
0.18V
0.09V
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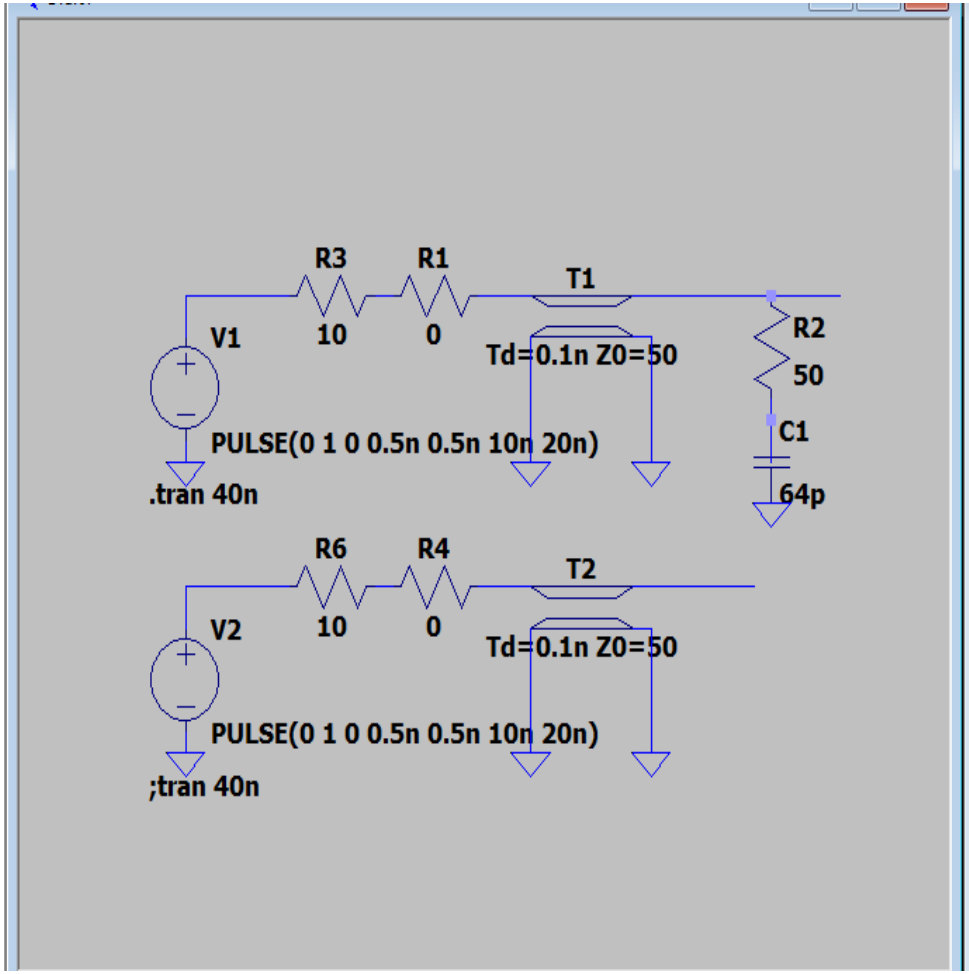
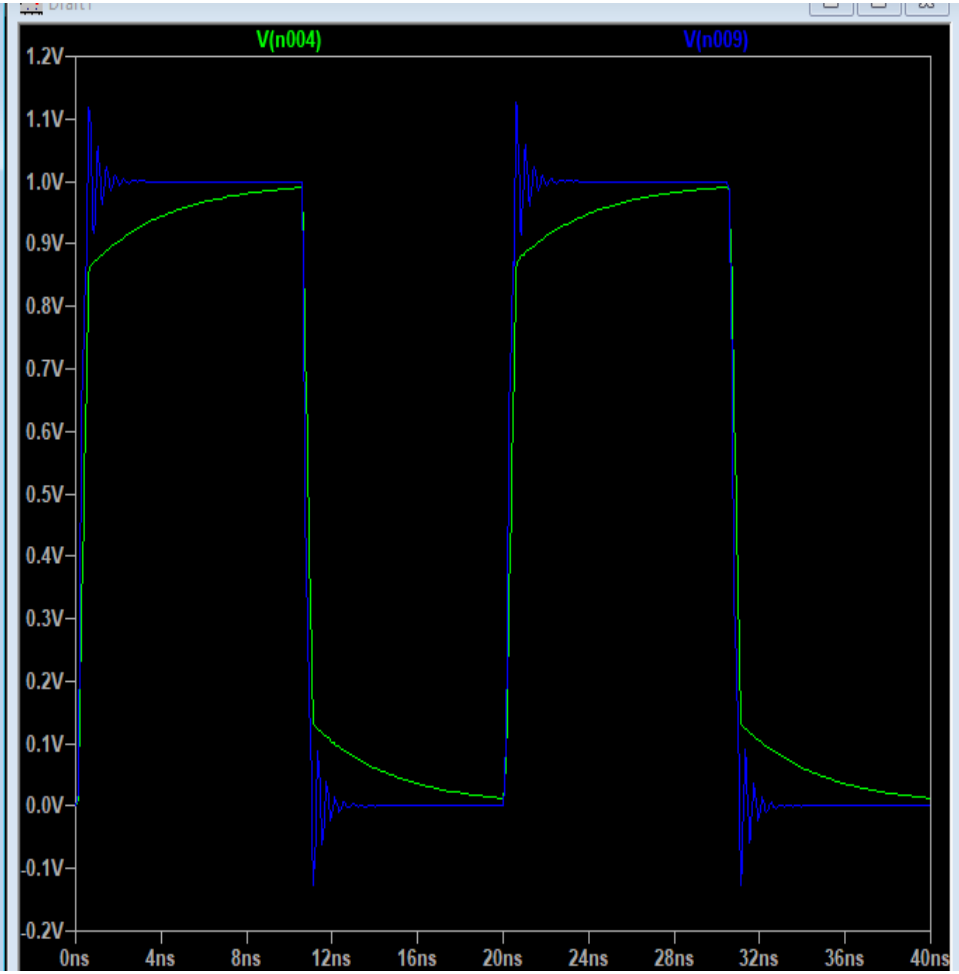
Series-RC parallel termination





REFLECTIONS FROM SHORT SERIES TRANSMISSION LINES

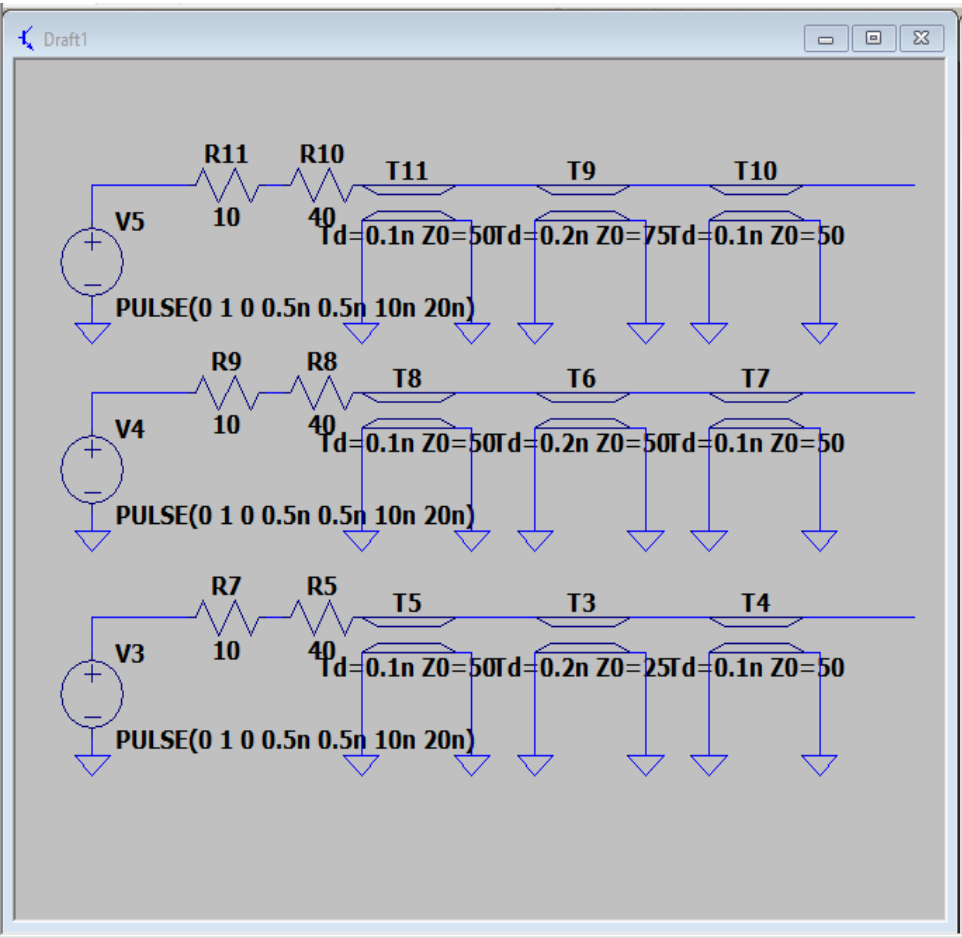
- Many times, the line width of an interconnect on a board must neck down, as it might in going through a via field or routing around a congested region of the board.
- If the line width changes for a short length of the line, the characteristic impedance will change, typically increasing.

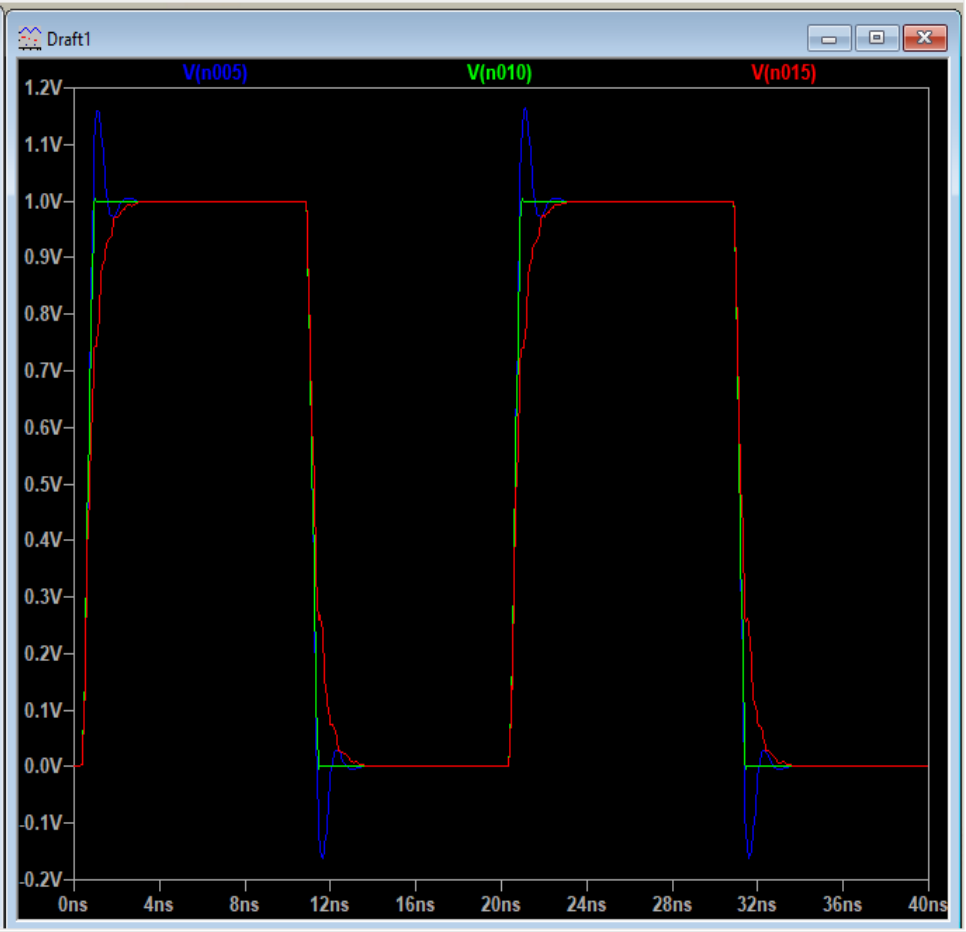
How much change in impedance and over what length might start to cause a problem?

- Three features determine the impact from a short transmission line segment:

T_D, Zo, and R_T

- When the time delay is long compared to the rise time—in other words, the discontinuity is electrically long—the reflected voltage will saturate.

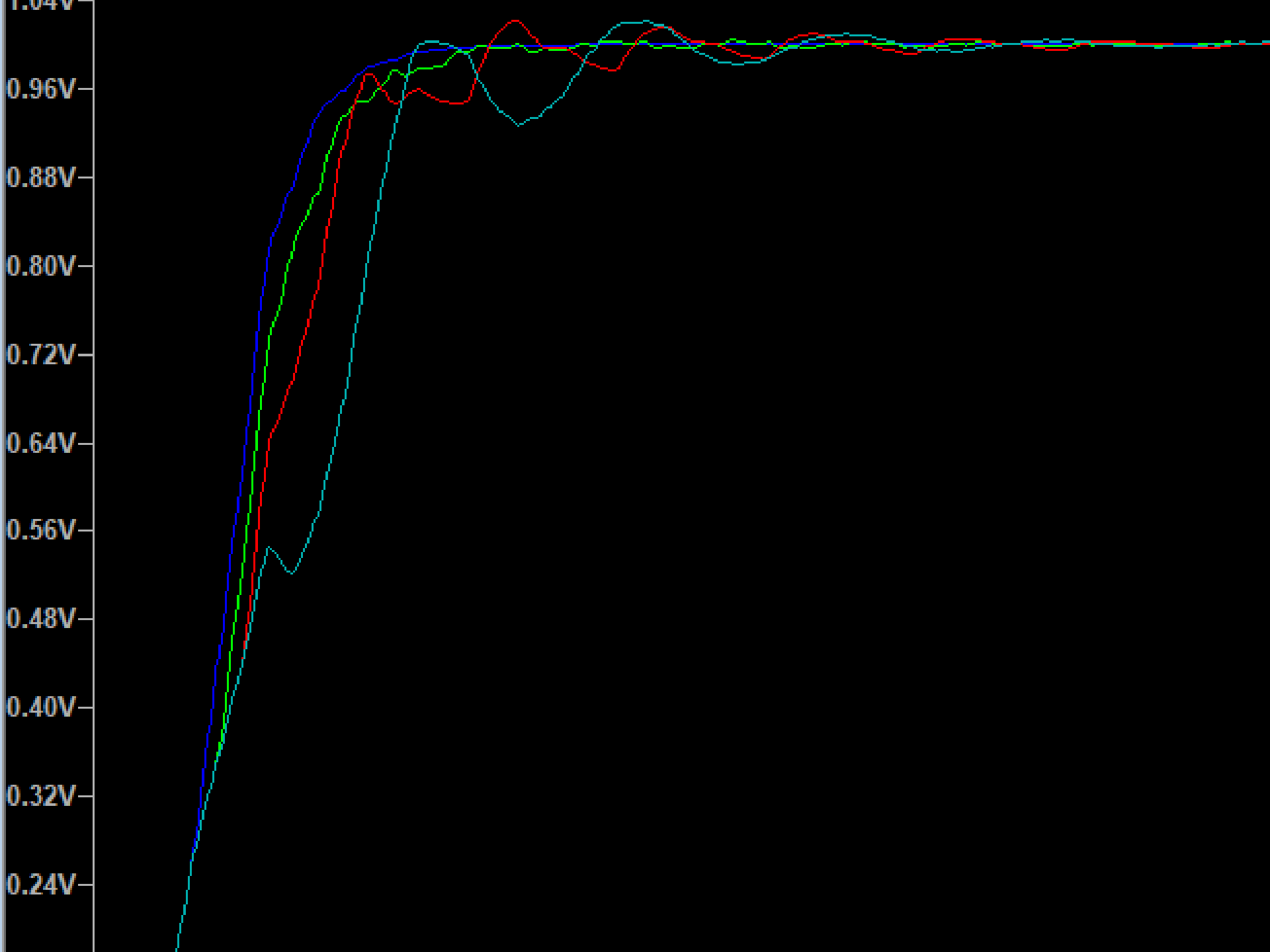

Draft1
R11
R10
T11
T9
T10
V5
10
40
Td=0.1n Z0=50
Td=0.2n Z0=75
Td=0.1n Z0=50
PULSE(0 1 0 0.5n 0.5n 10n 20n)
R9
R8
T8
T6
T7
V4
10
40
Td=0.1n Z0=50
Td=0.2n Z0=50
Td=0.1n Z0=50
PULSE(0 1 0 0.5n 0.5n 10n 20n)
R7
R5
T5
T3
T4
V3
10
40
Td=0.1n Z0=50
Td=0.2n Z0=25
Td=0.1n Z0=50
PULSE(0 1 0 0.5n 0.5n 10n 20n)


Draft1
V(n005)
V(n010)
V(n015)
1.2V
1.1V
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
-0.1V
-0.2V
0ns
4ns
8ns
12ns
16ns
20ns
24ns
28ns
32ns
36ns
40ns

REFLECTIONS FROM SHORT-STUB TRANSMISSION LINES

- A branch is added to a uniform transmission line to allow the signal to reach multiple fanouts.
- When the branch is short, it is called a *stub*.
- A stub is commonly found on BGA packages.
- The two important factors that determine the impact of the stub on signal quality are the **rise time** of the signal and the **length of the stub**.

$$\mathrm{Len}_{\mathrm{stub-max}}\,[\mathrm{inches}] < \mathrm{RT}\,[\mathrm{n\,sec}]$$


1.04V
0.96V
0.88V
0.80V
0.72V
0.64V
0.56V
0.48V
0.40V
0.32V
0.24V

REFLECTIONS FROM CAPACITIVE END TERMINATIONS

- All real receivers have some **input-gate capacitance**.
- The receiver's package-signal lead might have a **capacitance to the return path**.
- When a signal travels down a transmission line and **hits an ideal capacitor at the end**.
- The actual instantaneous impedance the signal sees, which determines the reflection coefficient, will change with time.
- The **impedance of a capacitor**, in the time domain, is related to:

$$Z = \frac{V}{C\frac{dV}{dt}}$$

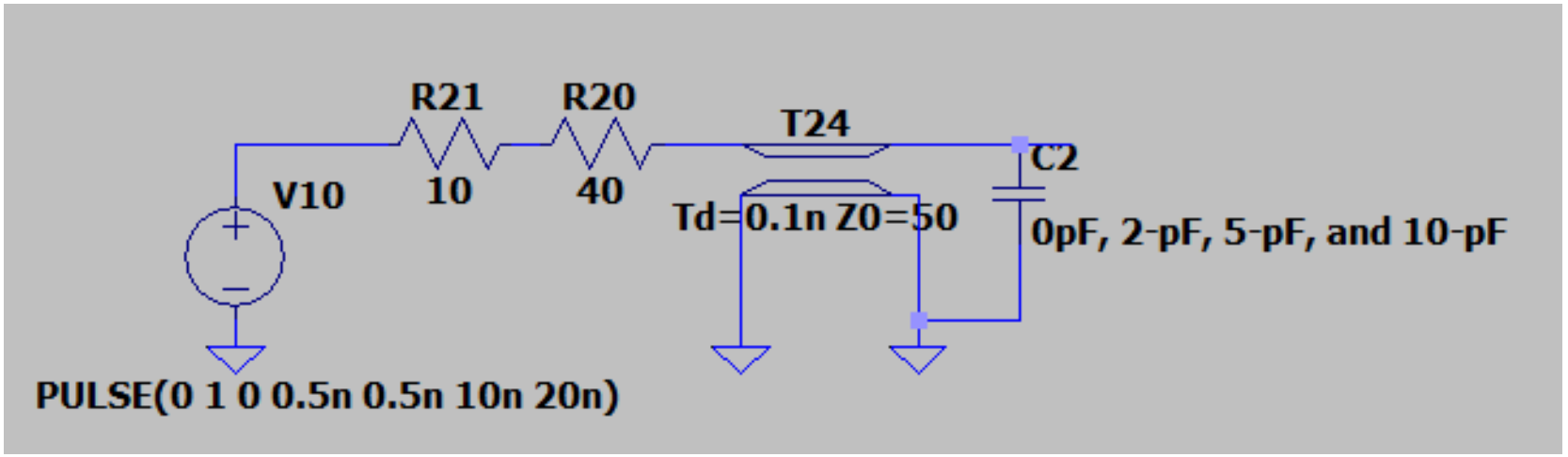
- If **the rise time** is short compared with the charging time of the capacitor,

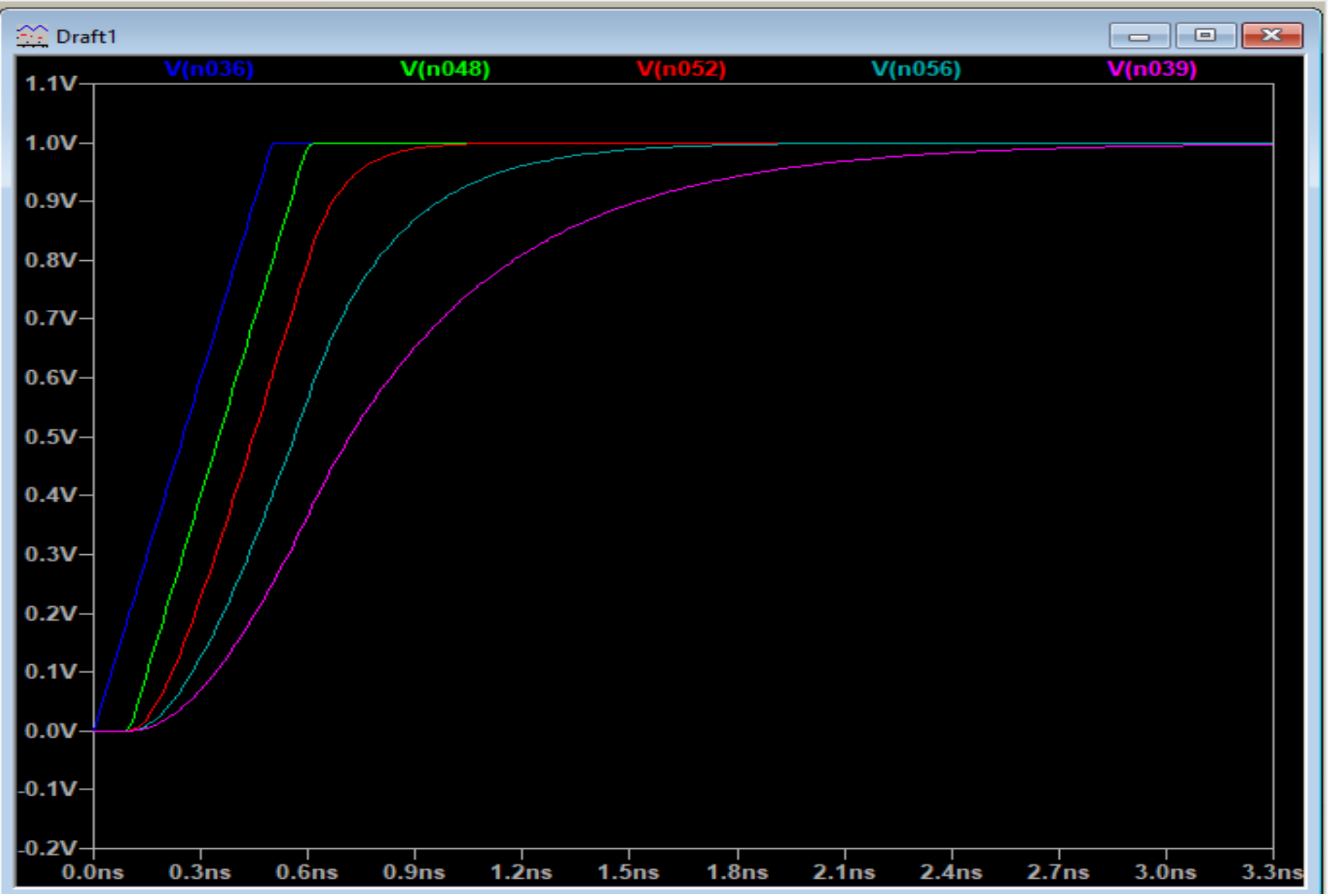
then initially, the **voltage will rise very quickly**, and Z will be low.

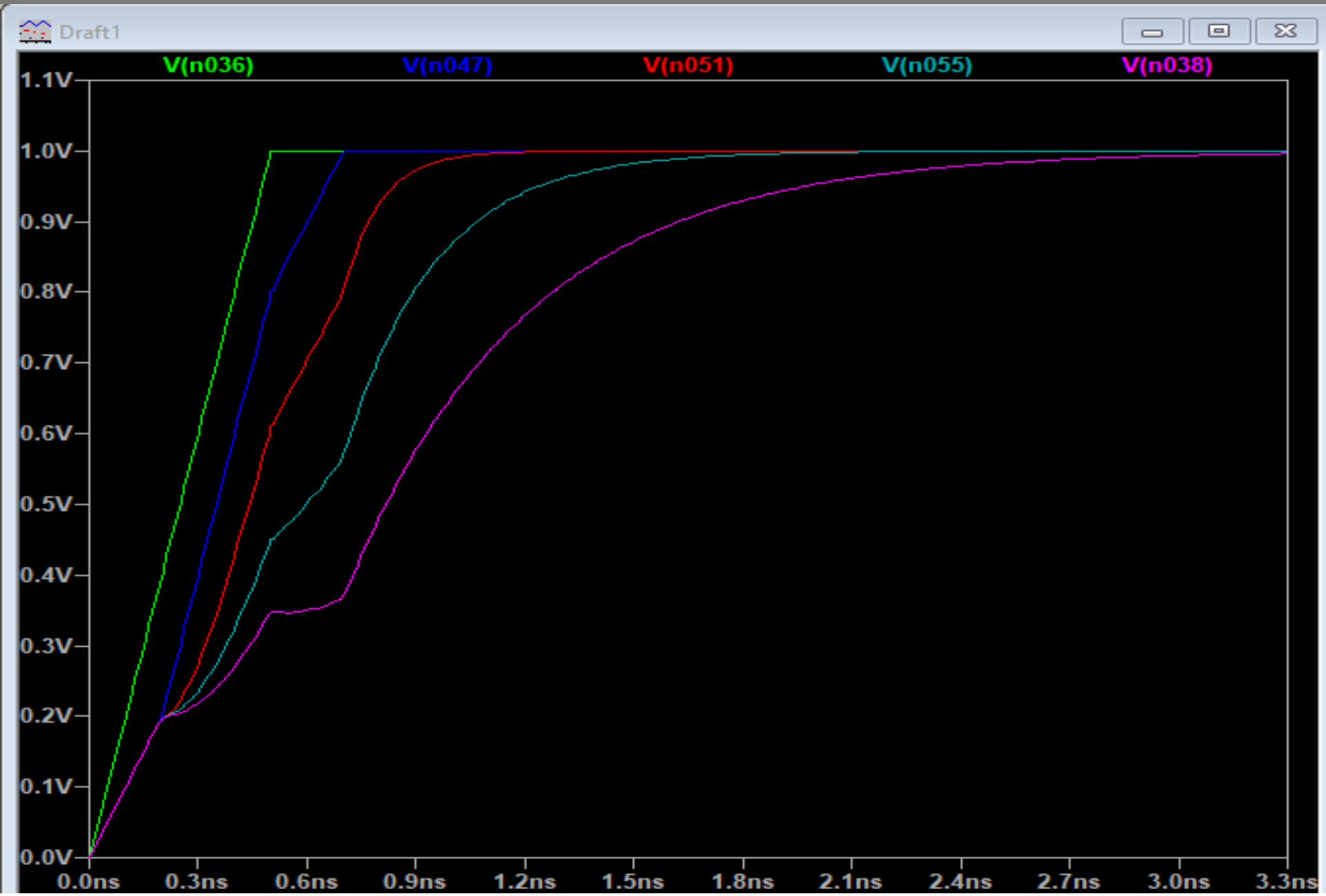
- But as the capacitor charges, the **voltage across it gets smaller**, and the **dV/dt slows down.**
- As the **capacitor charges up**, the rate at which the voltage across it changes will slow down.
- This will cause **the impedance of the capacitor** to increase dramatically.
- If we wait long enough, **the impedance of a capacitor**, after it has charged fully, is open.

REFLECTIONS FROM CAPACITIVE END TERMINATIONS

- This means the reflection coefficient will change with time.
- The reflected signal should suffer a dip and then move up to look like an open.
- The exact behavior will depend on the characteristic **impedance of the line (Z), the capacitance of the capacitor**, and **the rise time** of the signal.
- The simulated reflected and transmitted voltage behavior for 2-pF, 5-pF, and 10-pF capacitances.




Draft1
V(n036)
V(n048)
V(n052)
V(n056)
V(n039)
1.1V
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
-0.1V
-0.2V
0.0ns
0.3ns
0.6ns
0.9ns
1.2ns
1.5ns
1.8ns
2.1ns
2.4ns
2.7ns
3.0ns
3.3ns

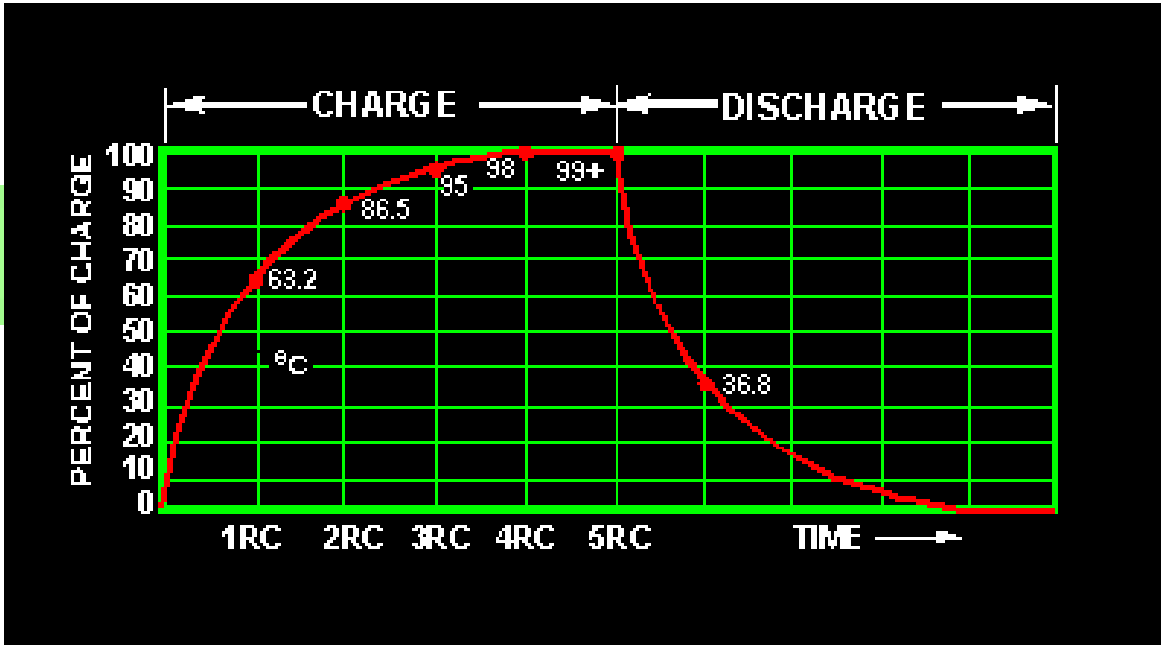

Draft1
V(n036)
V(n047)
V(n051)
V(n055)
V(n038)
1.1V
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
0.0ns
0.3ns
0.6ns
0.9ns
1.2ns
1.5ns
1.8ns
2.1ns
2.4ns
2.7ns
3.0ns
3.3ns

REFLECTIONS FROM CAPACITIVE END TERMINATIONS

- The long-term response of the transmitted voltage pattern looks like the charging of a capacitor by a resistor.
- The presence of the capacitor filters the rise time and acts as a **"delay adder"** for the signal at the receiver.
- It is very similar to the charging of an RC circuit. $\tau_e = R \times C$
- The 10% -90% rise time is related to the RC time constant by:

$$\tau_{10-90} = 2.2 \times \tau_e = 2.2 \times R \times C$$

$$\tau_{10-90} = 2.2 \times Z_0 \times C$$



REFLECTIONS FROM CAPACITIVE END TERMINATIONS

- For example, if Zo=50 Ohms C=10 pF, the 10-90 charging time will be 2.2 × 50 Ohms × 10 pF = 1.1 nsec.

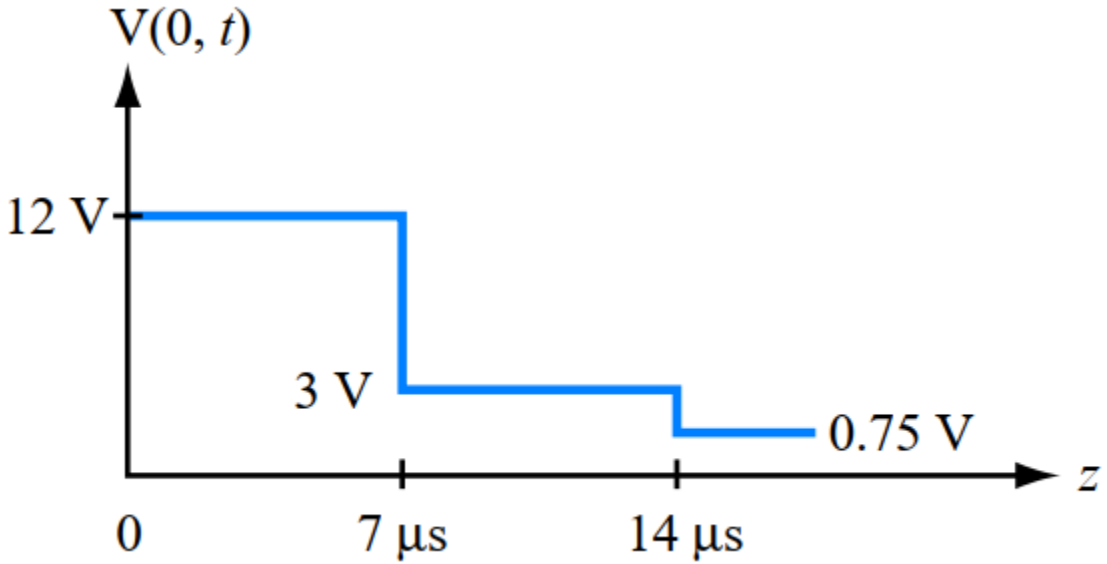
- If the initial-signal rise time is **short compared** with this 1.1-nsec charging time, the presence of the capacitive load at the end of the line will dominate and will now determine the rise time at the receiver.

- If the initial rise time of the signal is **long compared** to the 10-90 charging rise time, the capacitor at the end will add a delay to the rise time, and it will be roughly equal to the 10-90 rise time.

Examples:

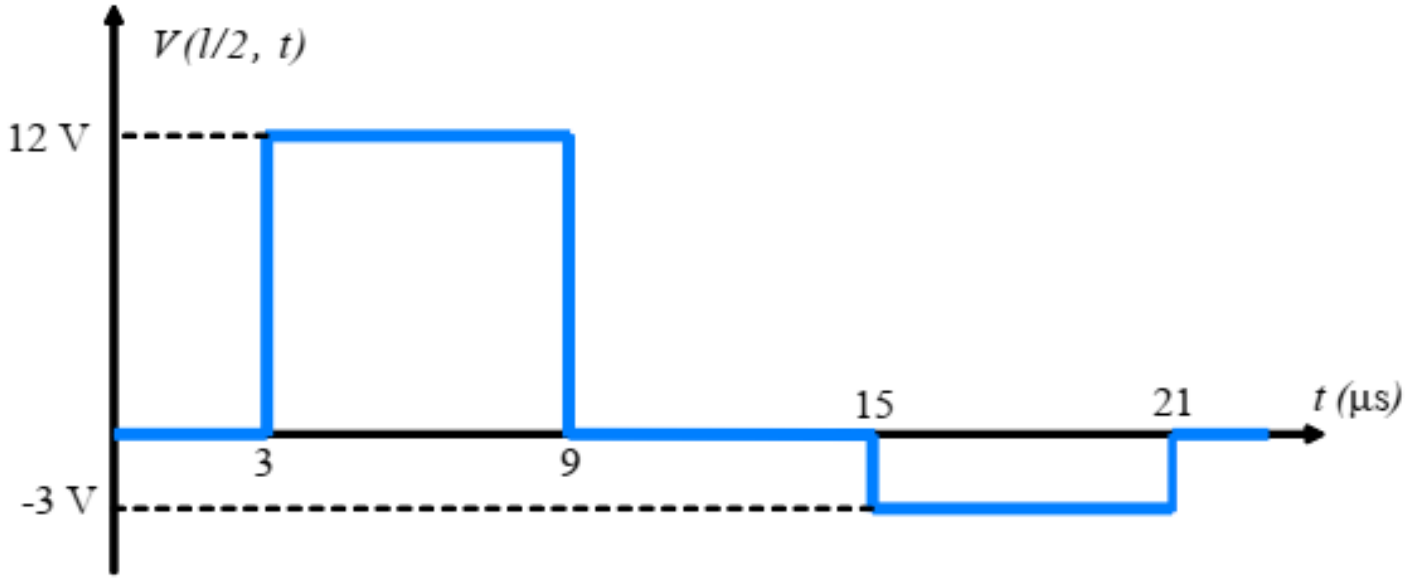
- In response to a step voltage, the voltage waveform shown in figure below, was observed at the sending end of a **shorted line** with $Z0 = 50$ ohms and

  $\varepsilon r = 4$. Determine Vg, Rg, and the line length of first change.



Example 2

- In response to a step voltage, the voltage waveform shown in the figure below was observed at the midpoint of a lossless transmission line with $Z0$ 50 ohms and up = 2 10^8 m/s. Determine: **(a)** the length of the line, **(b)** ZL, **(c)** Rg, and **(d)** Vg.



Example 3

- If the output impedance of a driver is 35 Ohms, what value of source-series resistor should be used in the driver when connected to

1. a 50-Ohm line?
2. a 65-Ohm line?

References

- **Signal and Power Integrity - Simplified by Eric Bogatin.**
- **FUNDAMENTALS OF APPLIED ELECTROMAGNETICS by Fawwaz T. Ulaby**

Budapest University of Technology and Economic
Department of Electron Devices

Circuit Environment

Lecture 10

Signal Integrity III

Cross-talk

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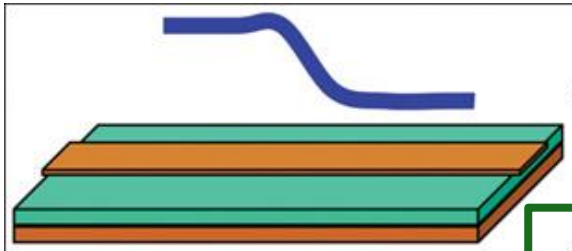
Sal-abassi@edu.bme.hu

2021/2022

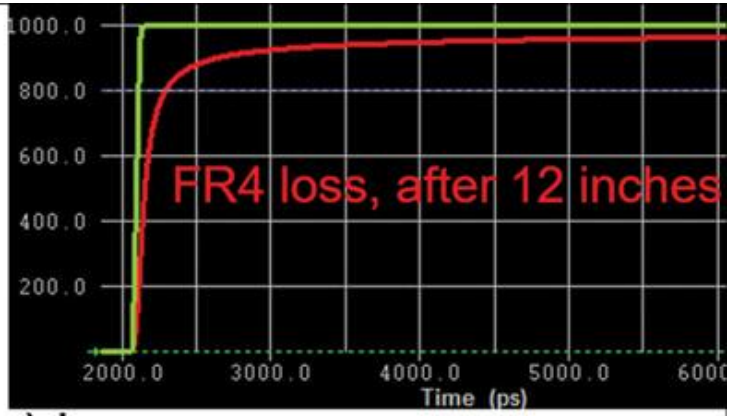
Cross Talk in Transmission Lines

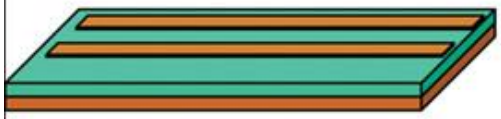
- Cross talk is one of the six families of signal-integrity problems.



1. Reflection noise

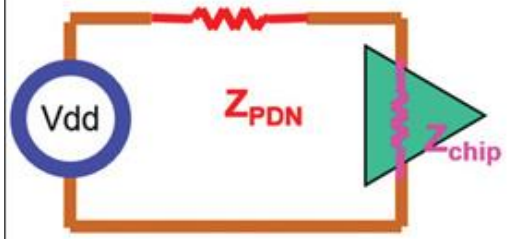
2. Cross talk





3. Ground (and power) bounce

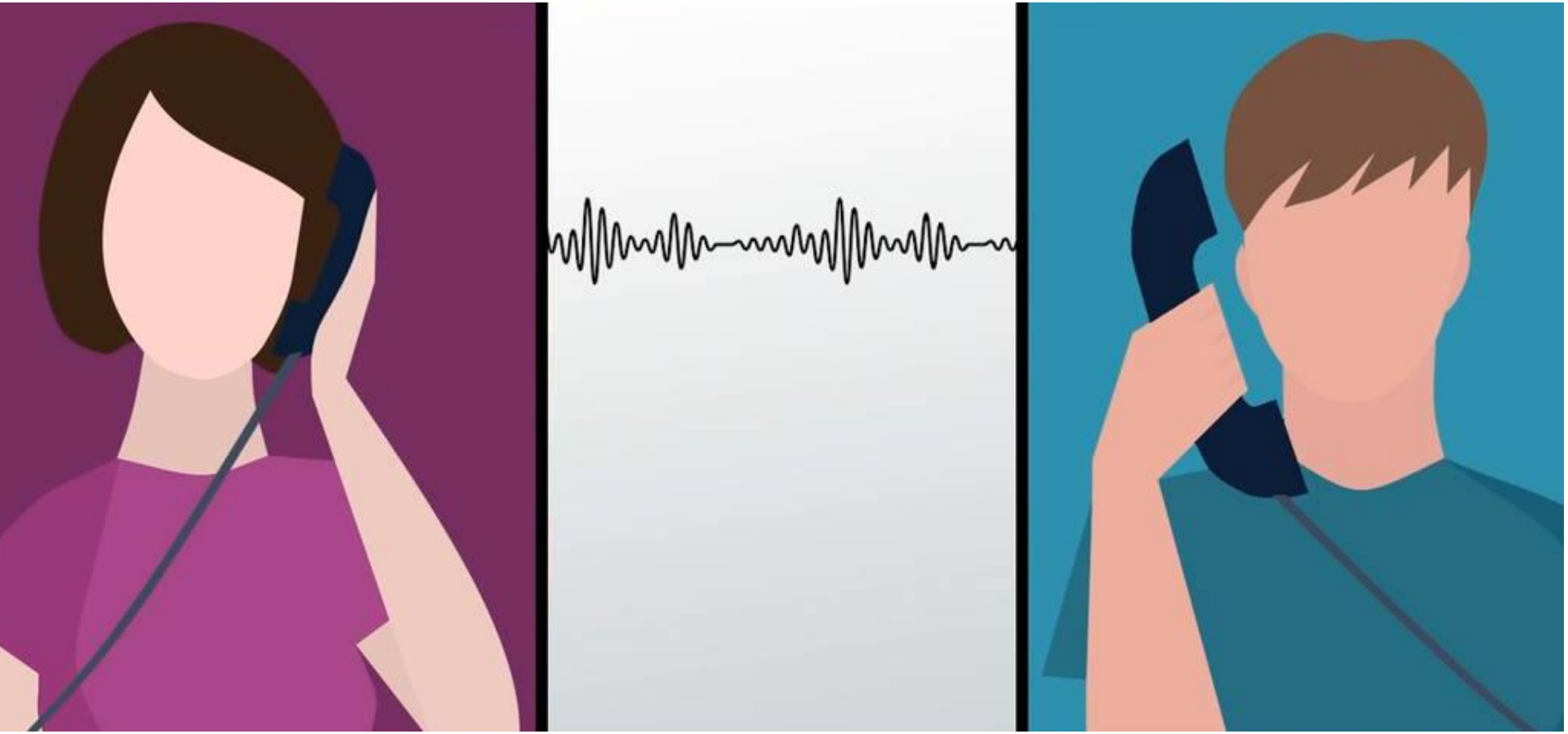
4. Losses (@ Gbps)



5. Rail collapse, voltage droop, power supply noise

6. EMI

The term Crosstalk comes from the early analog phone lines where you could actually hear voices from neighboring lines due to EM coupling.



Cross Talk in Transmission Lines

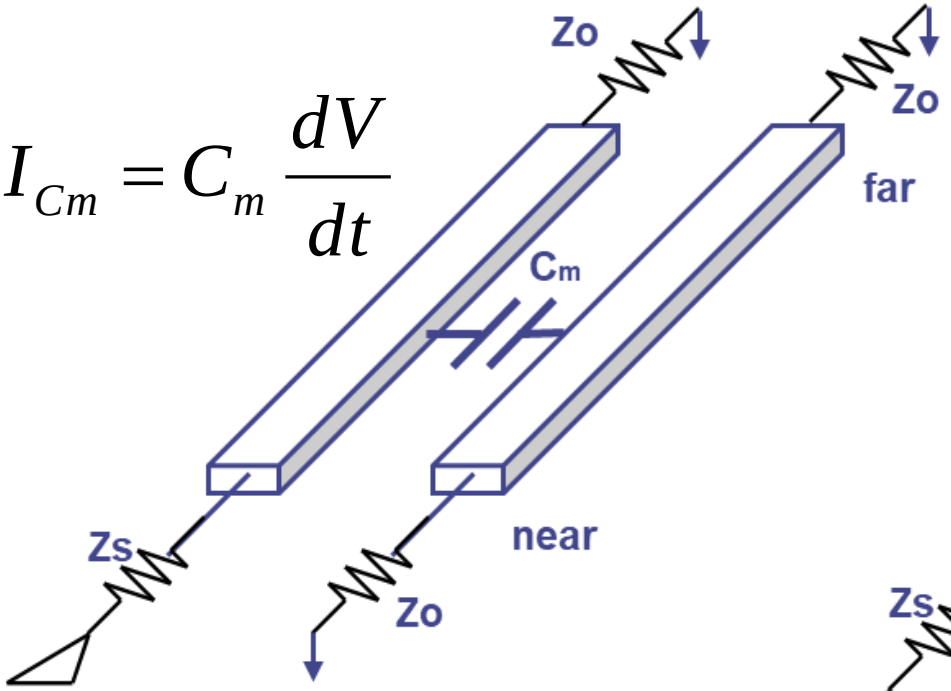
- It is the transfer of an **unwanted signal** from one net to an adjacent net, and it occurs between every pair of nets.
- A net includes both the **signal and the return path**, and it connects one or more nodes in a system.
- We typically call the net with the source of the noise **the *active net* or the *aggressor net*.**
- The net on which the noise is generated is called **the *quiet net* or the *victim net*.**
- **The noise margin is typically about 15%** of the total signal-voltage swing, but it varies among device families.
- Of this 15%, about one-third, or **5%,** of the signal swing is typically allocated to **cross talk.**
- If the signal swing were 3.3 v, the maximum allocated cross talk might be about 160 mV.
- This is a good starting place for the **maximum allowable cross-talk noise**.

Crosstalk

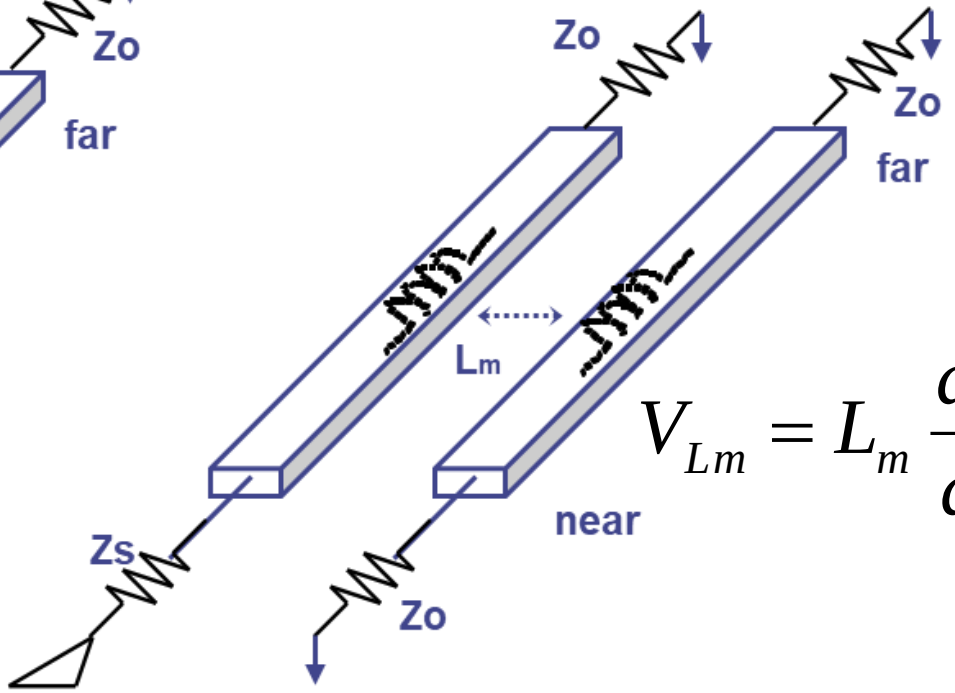
- The Crosstalk can be due to **Electric or Magnetic Field lines** interacting with a neighboring line.

Mutual Capacitance, C_m

$$I_{Cm} = C_m \frac{dV}{dt}$$

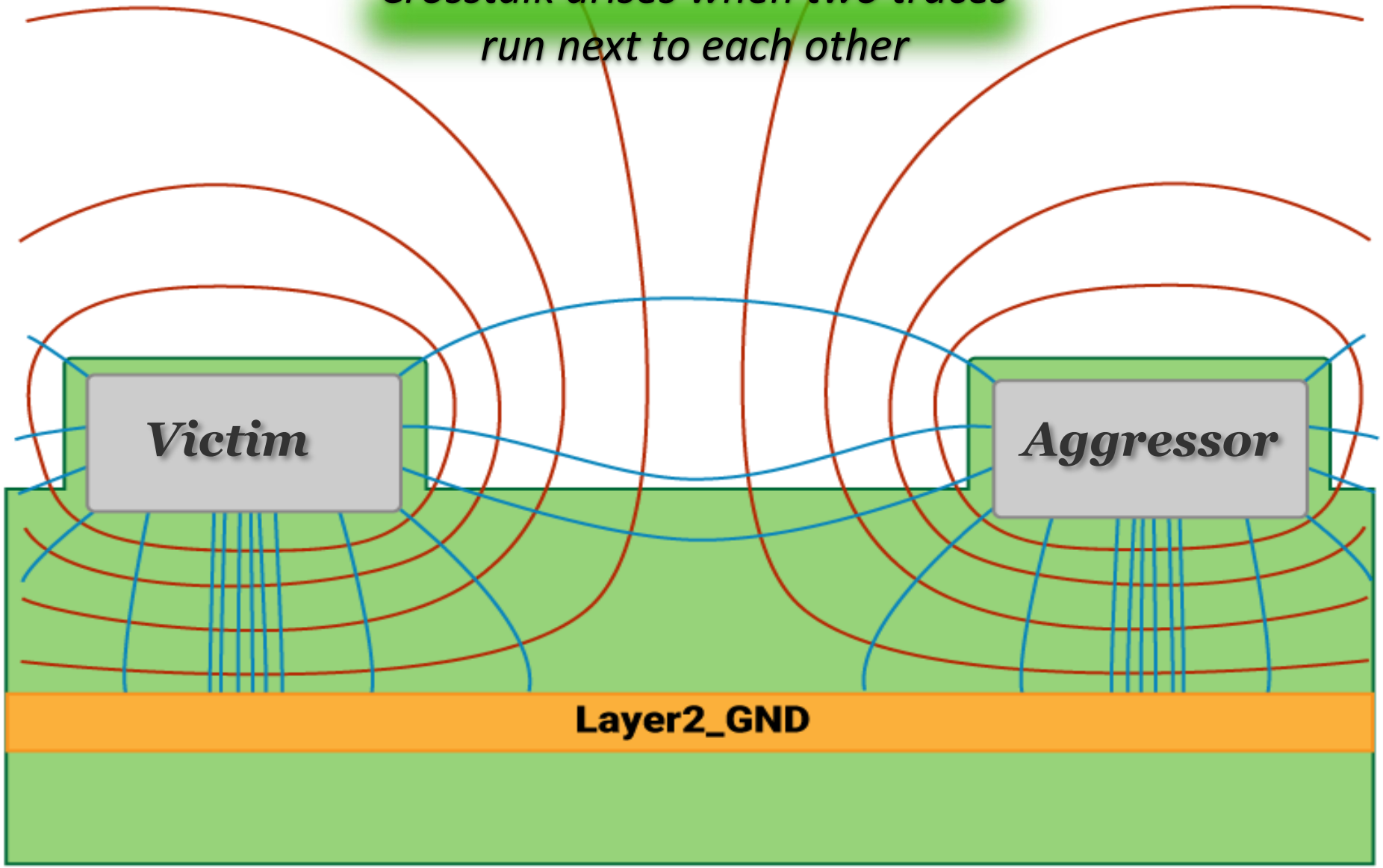


Mutual Inductance, L_m



$$V_{Lm} = L_m \frac{dI}{dt}$$

Crosstalk arises when two traces run next to each other



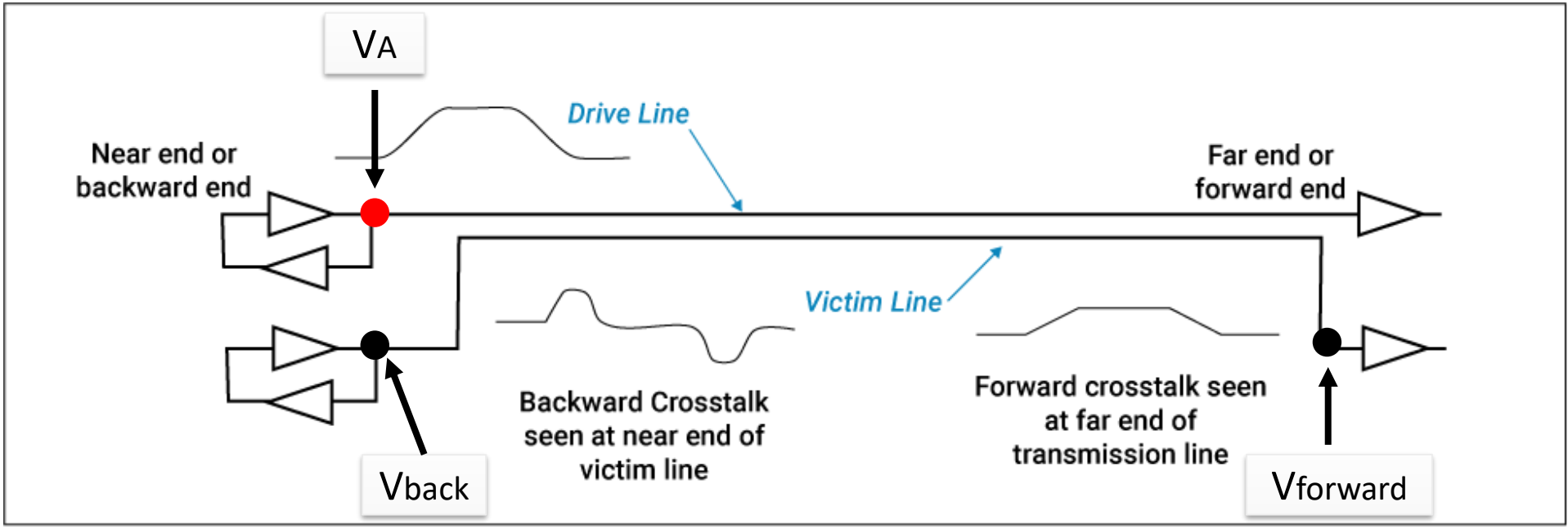
Crosstalk Classes: There are two main classes of crosstalk

1. **Signal crosstalk**
   - When C_M and L_M produce crosstalk noise on **the same order of magnitude**
   - When **the signal path** is the reason for the crosstalk
   - This is what we see on **PCB's** and **on-chip** traces
2. **Switching Noise**
   - When the **return path** is **highly inductive**, and the inductive noise dominates
   - When the inductance in **the return path** is the reason for the crosstalk
   - This is what we see on **packages** and in **connectors**
   - This is also called:

"Ground Bounce / Power Supply Droop"
"Simultaneous Switching Noise (SSN)"
"Simultaneous Switching Output (SSO) Noise"

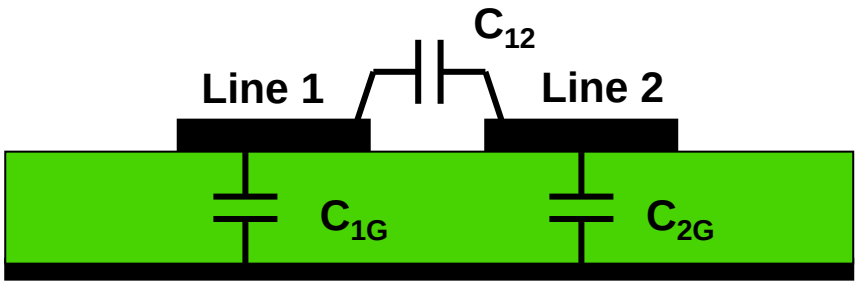
Crosstalk Location:

- There are two locations where we observe and define crosstalk
  - Near End - the location closest to the driving source resistor
  - Far End - the location closest to the receiving termination resistor
  - NEXT - Near End Crosstalk Coefficient (V_{back}/V_A)
  - FEXT - Far End Crosstalk Coefficient ($V_{forward}/V_A$)

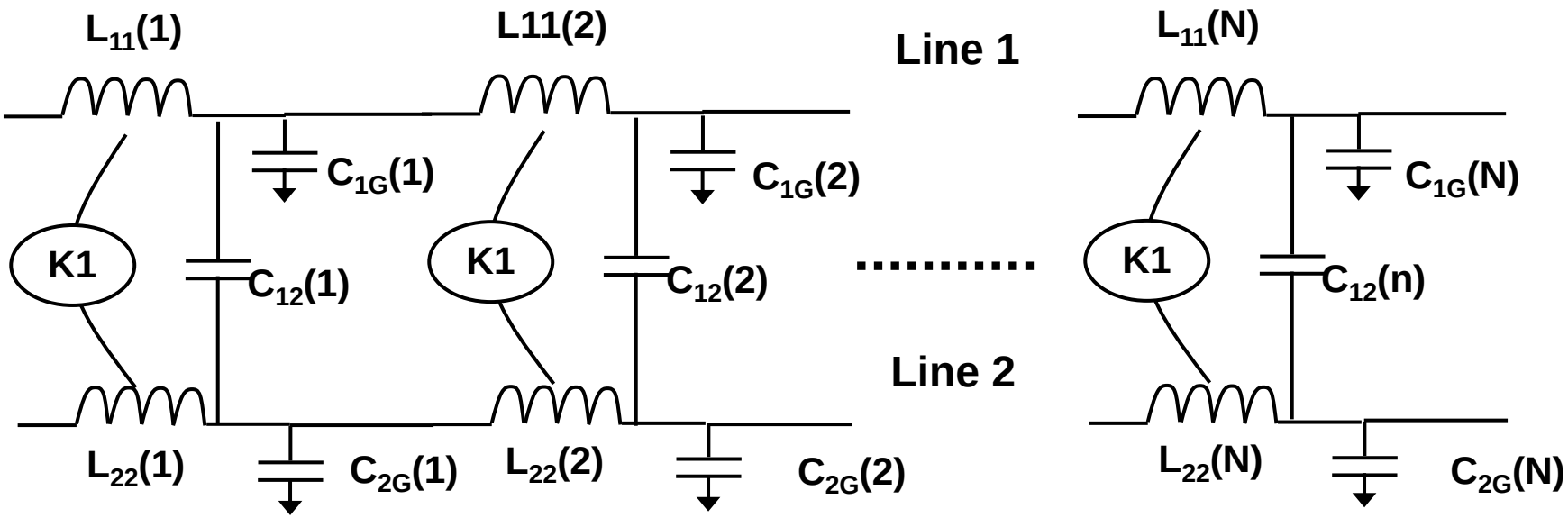


Creating a Crosstalk Model:

- *The circuit must be distributed into N segments as shown in chapter 2*

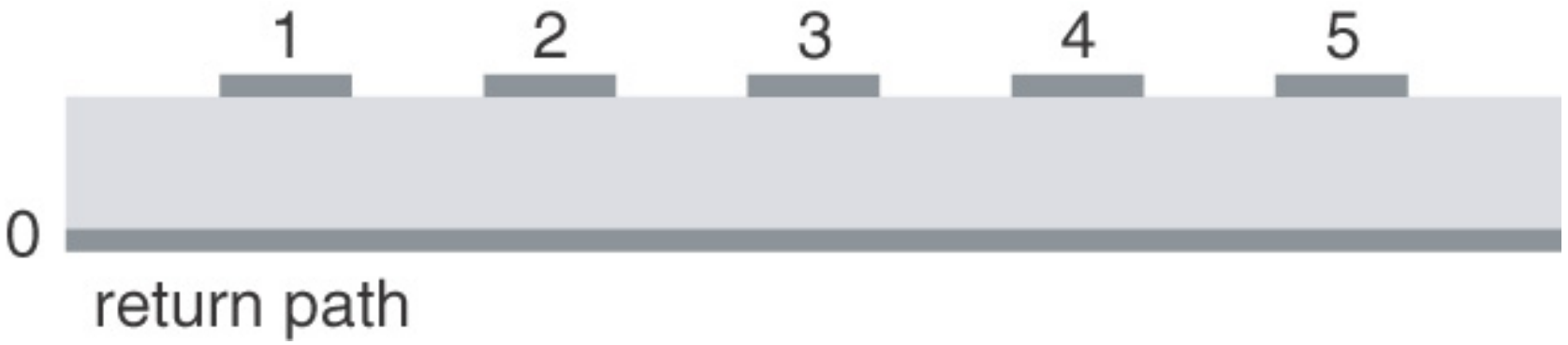


$$K = \frac{L_{12}}{\sqrt{L_{11}L_{22}}}$$

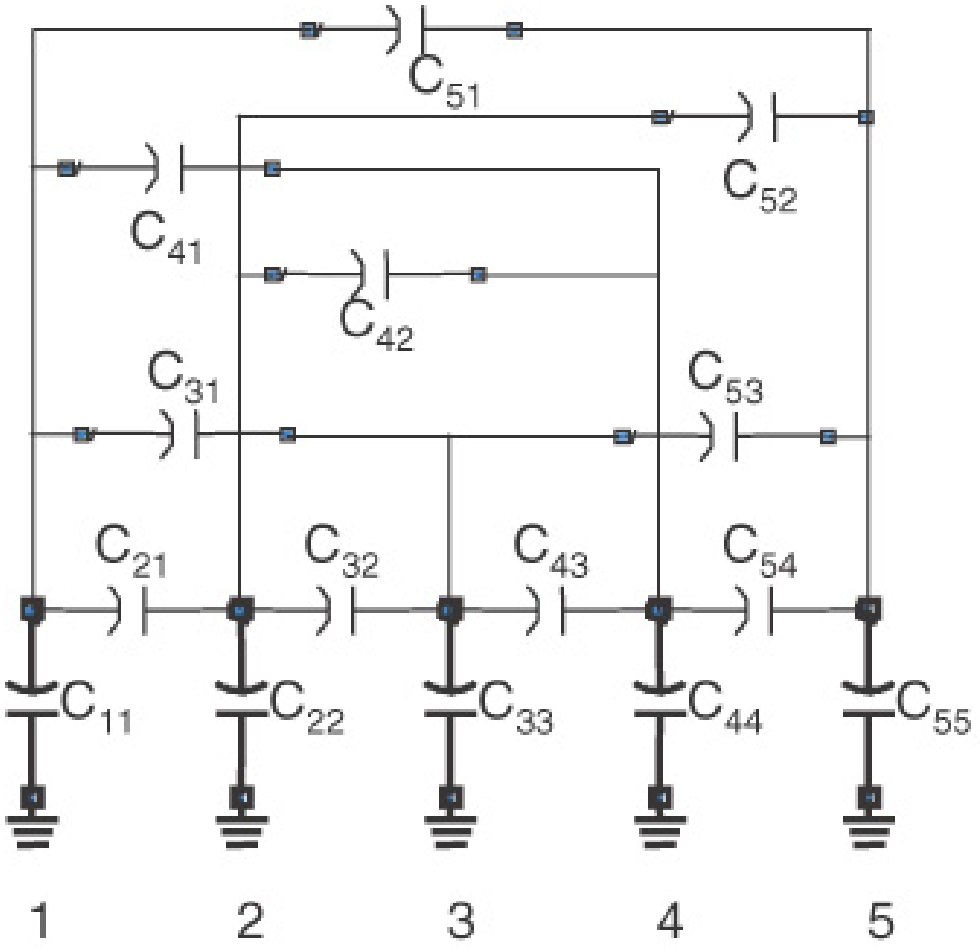


THE SPICE CAPACITANCE MATRIX:

- There can be multiple signal lines in a system.
- To keep track of their LC values, we use a matrix.
- Each signal is given an index, where ground is "0“
- Define C11 as the self capacitance of signal 1 (and also for C22, C33, etc…).
- Define C12 as the mutual capacitance between signals 1 and 2 (and also for C13, C23, etc.…).
- In this system, C12 and C21 are equal.
- Then put all the values in a Matrix for easy record keeping.
- Do the same for the Inductances

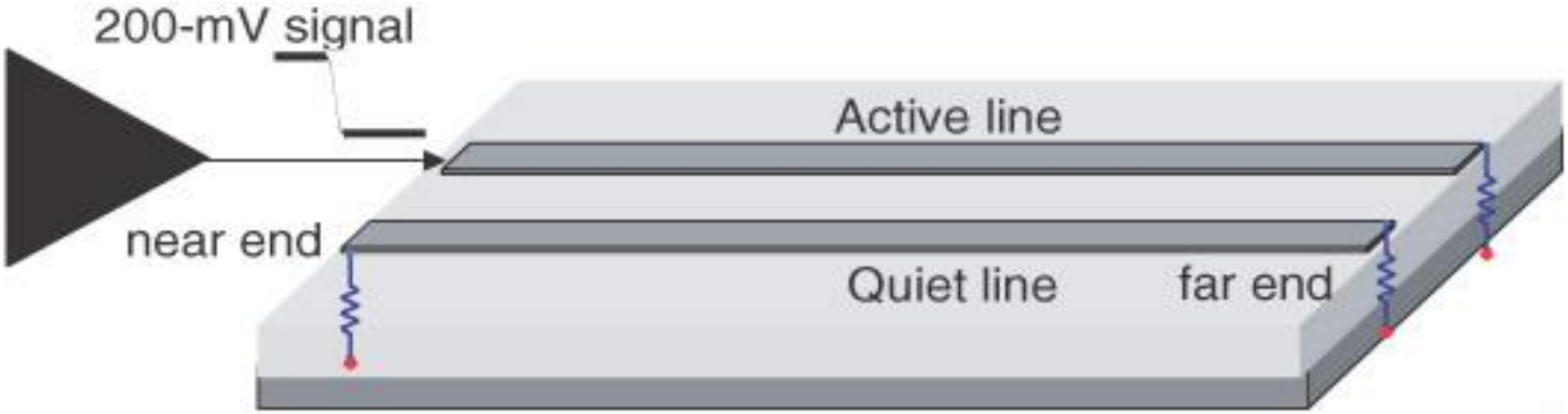


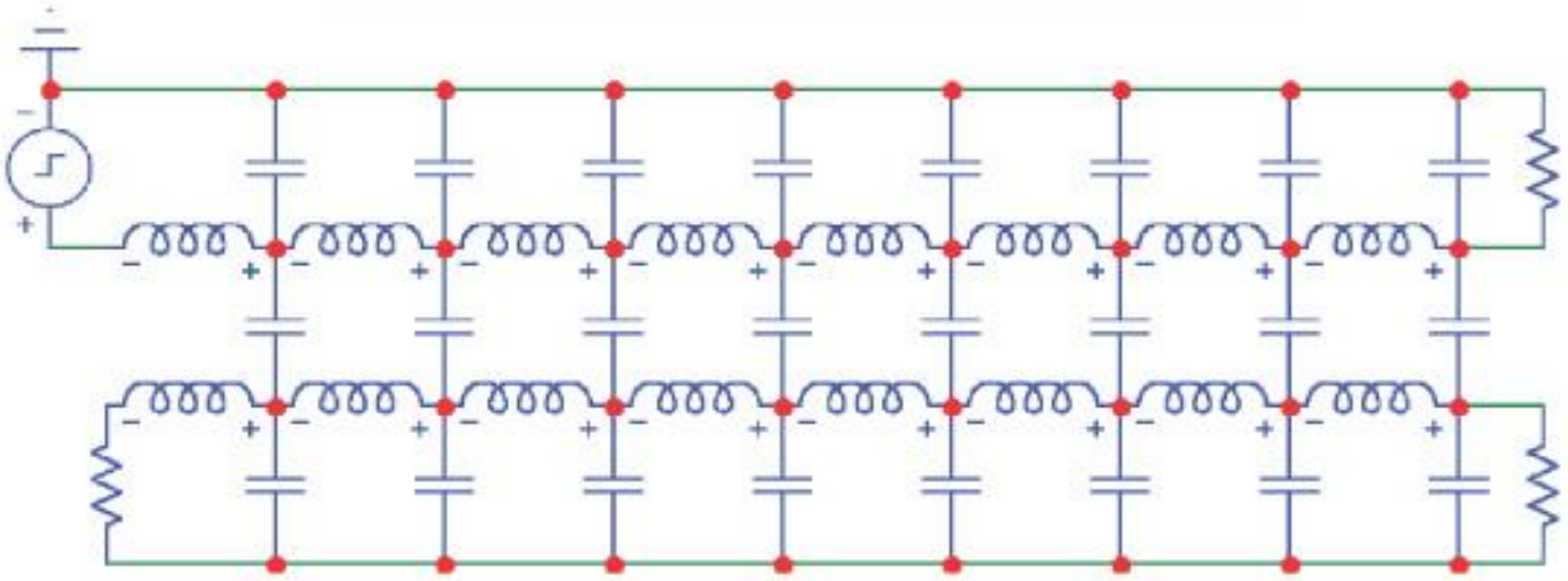
Capacitance Network:



$$\begin{matrix} C_{11} & C_{12} & C_{13} & C_{14} & C_{15} \\ C_{21} & C_{22} & C_{23} & C_{24} & C_{25} \\ C_{31} & C_{32} & C_{33} & C_{34} & C_{35} \\ C_{41} & C_{42} & C_{43} & C_{44} & C_{45} \\ C_{51} & C_{52} & C_{53} & C_{54} & C_{55} \end{matrix}$$

Transmission lines and an equivalent circuit model:

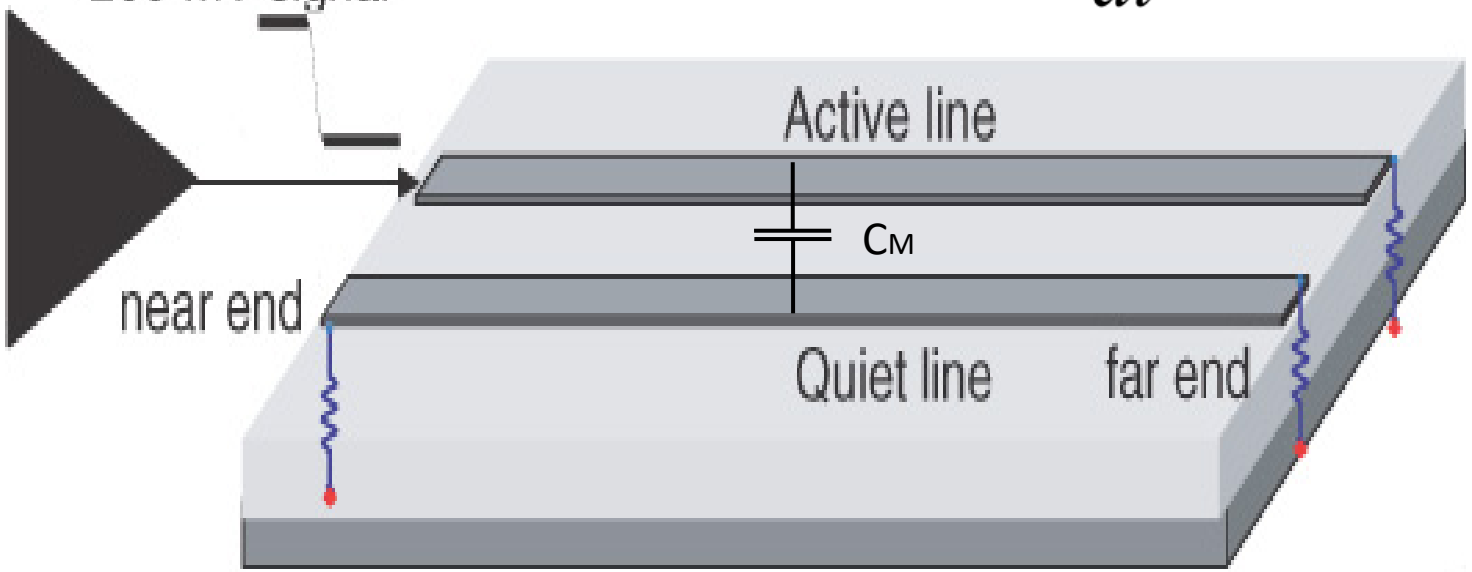




Capacitive Crosstalk:

- As the Aggressor Edge propagates down the line, it will inject current into the Victim line through the Mutual Capacitance.
- **The rising edge** will act as a current source moving down the active line. **Why?**

$$I_C = C_M \frac{dV}{dt}$$



Capacitive Crosstalk:

- The current will equally split and half will travel forward and half will travel backwards. **Why?**
- The total amount of current injected at any given time is related to the spatial extent of the risetime.
- This can be described using the per unit length value for Mutual Capacitance (CM').

$$C_M = C_M' \cdot \Delta x$$

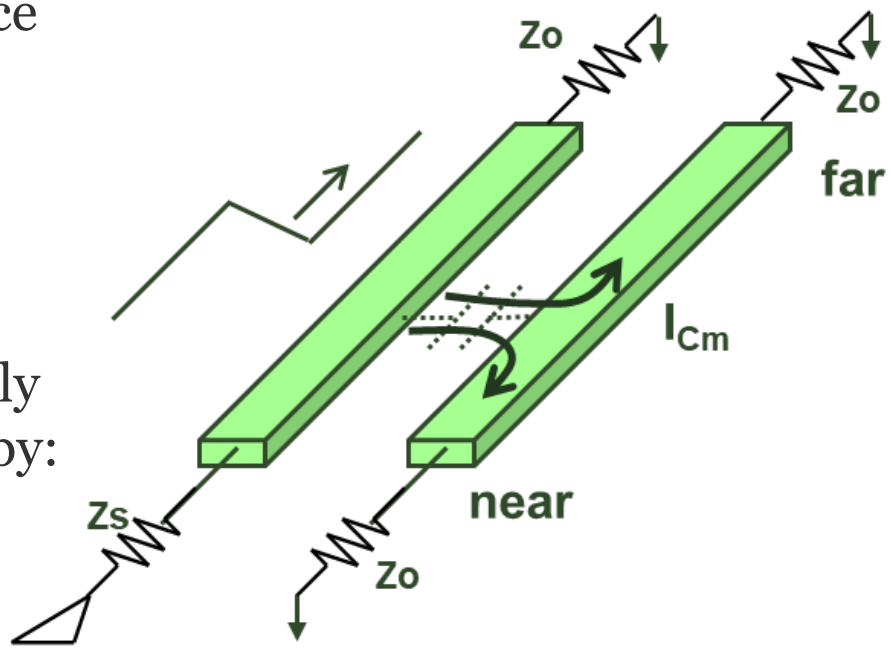
$$C_M = C_M' \cdot (vel \cdot t_{rise})$$

- The total amount of instantaneously injected current is then described by:

$$I_C = C_M \frac{dV}{dt}$$

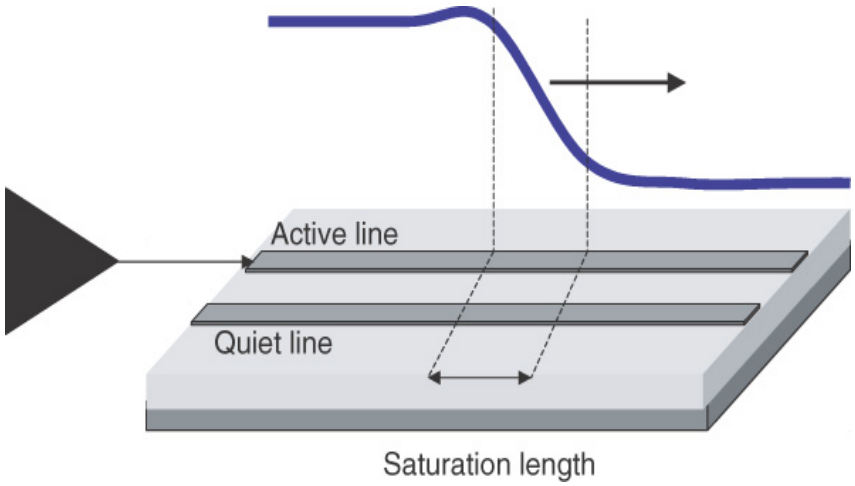
$$I_C = C_M' \cdot (vel \cdot t_{rise}) \cdot \left(\frac{V}{t_{rise}} \right)$$

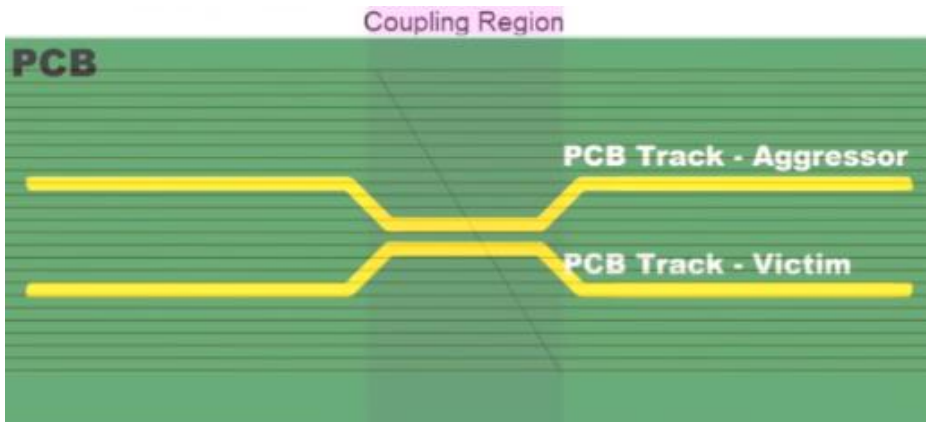
$$I_C = C_M' \cdot vel \cdot V$$



Capacitive Crosstalk: (Near End)

- Half of the current injected into the victim as the incidence voltage step travels down the aggressor travels back to the Near End.
- At any given time, only a fixed amount of current will be observed at the Near End.
- This means the Near End voltage will raise to a fixed value and remain there.
- At the point the aggressor edge reaches the end of the line (TD), the injected noise on the victim still needs to travel back to the Near-End (taking another TD).
- This means the fixed noise level at the Near End will remain for 2·TD





Capacitive Crosstalk: (Near End)

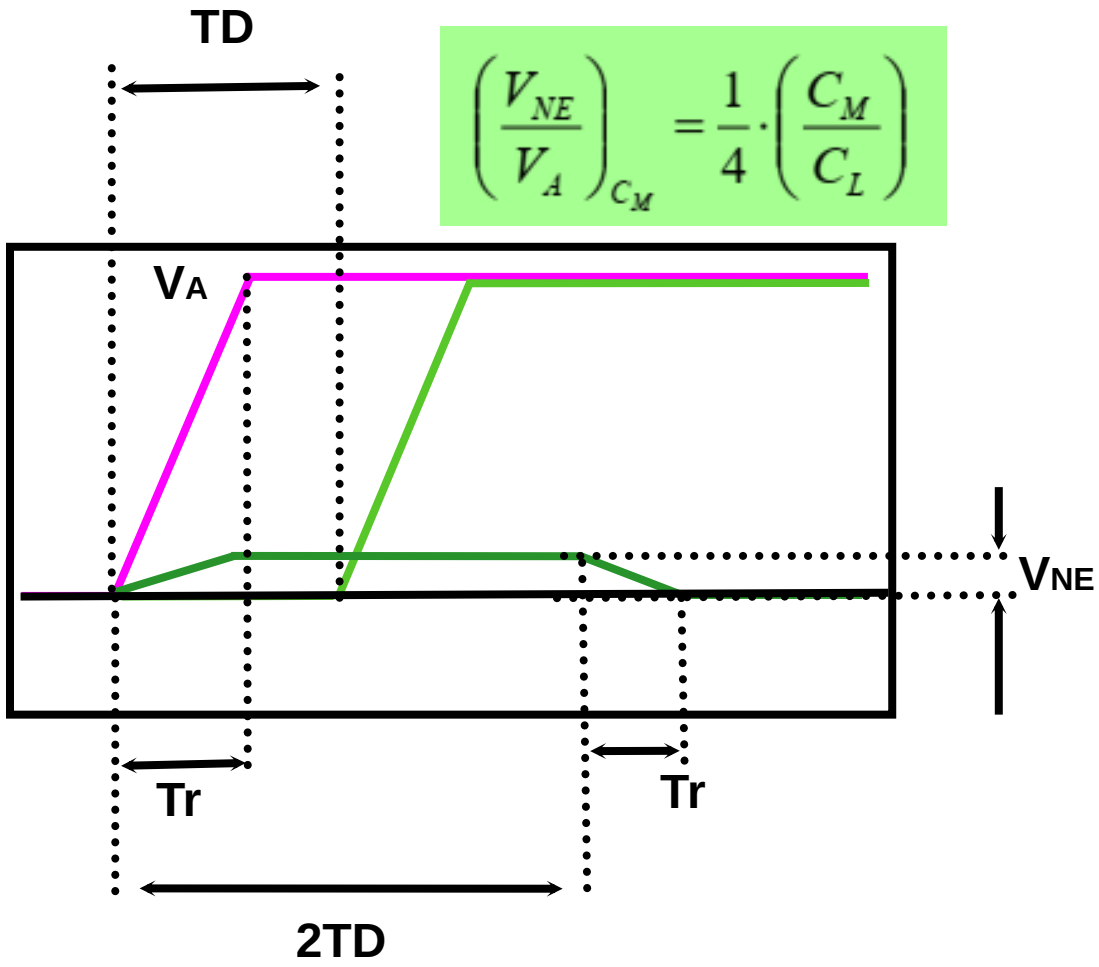
- After a time equal to the rise time, the current appearing at the near end will reach its peak value.
- After the beginning of the rising edge in the active line has left the coupled region and reached the far-end terminating resistor, the coupled-noise current will begin to decrease, taking a time equal to the rise time. There is still the backward-moving current in the quiet line that has yet to reach the near end of the quiet line.
- It will continue flowing back to the near end of the quiet line, taking
- additional time equal to the time delay, TD, of the coupled region.
- The signature of **the near-end**, capacitively coupled current is a rise up to a constant value in a time equal to the signal's rise time and staying at a constant value lasting for a time equal to 2 × TD – rise time.
- Then falling to zero in a rise time.

Capacitive Crosstalk: (Near End):

$$I_C = \left(\frac{1}{2}\right)\cdot\left(\frac{1}{2}\right)\cdot C_M{}'\cdot vel\cdot V = \left(\frac{1}{4}\right)\cdot C_M{}'\cdot vel\cdot V$$

The Near End Cross-talk due to Mutual Capacitance was derived and seen that the voltage rises to a constant level and remains there for 2·TD

$$\left(\frac{V_{NE}}{V_A}\right)_{C_M} = \frac{1}{4}\cdot\left(\frac{C_M}{C_L}\right)$$



Capacitive Crosstalk: (Far End)

- Now we look at the Noise observed at **the Far-End of the Victim line**.
- This noise is due to the forward traveling current that is injected through CM.

$$I_C = C_M \frac{dV}{dt}$$

$$I_C = C_M' \cdot (vel \cdot t_{rise}) \cdot \left(\frac{V}{t_{rise}} \right)$$

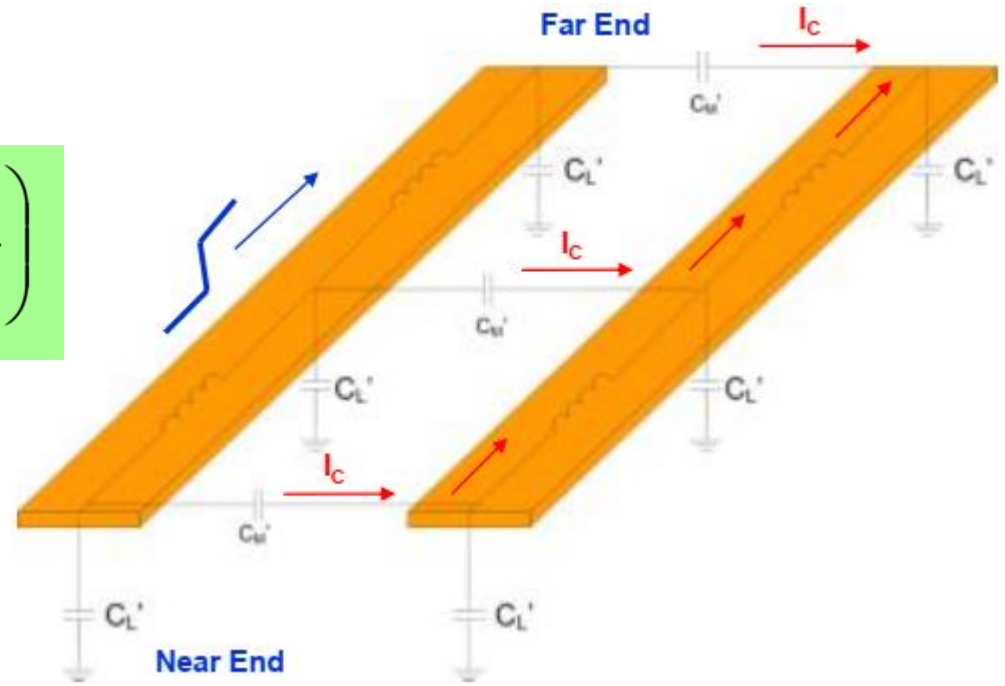
$$I_C = C_M' \cdot vel \cdot V$$

- 1/2 of this current travels forward toward the Far-End.
- The current noise is not seen until the Aggressor incident wave reaches the Far-End.
- Because the forward current in the quiet line is moving to the far end at exactly the same speed as the signal edge is moving to the far end in the active line.

Capacitive Crosstalk: (Far End)

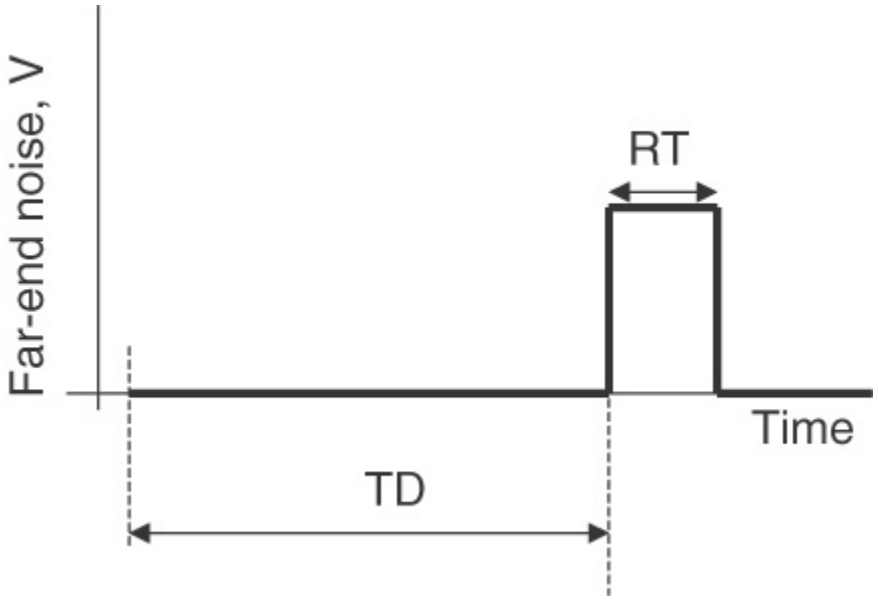
- Therefore, all the current that is injected into the victim line will add together and be injected into the last C_L segment of the Victim at the Far-End

$$\left(\frac{V_{FE}}{V_A}\right)_{C_M} = \frac{1}{2}\cdot\left(\frac{length}{vel\cdot t_{rise}}\right)\cdot\left(\frac{C_M}{C_L}\right)$$



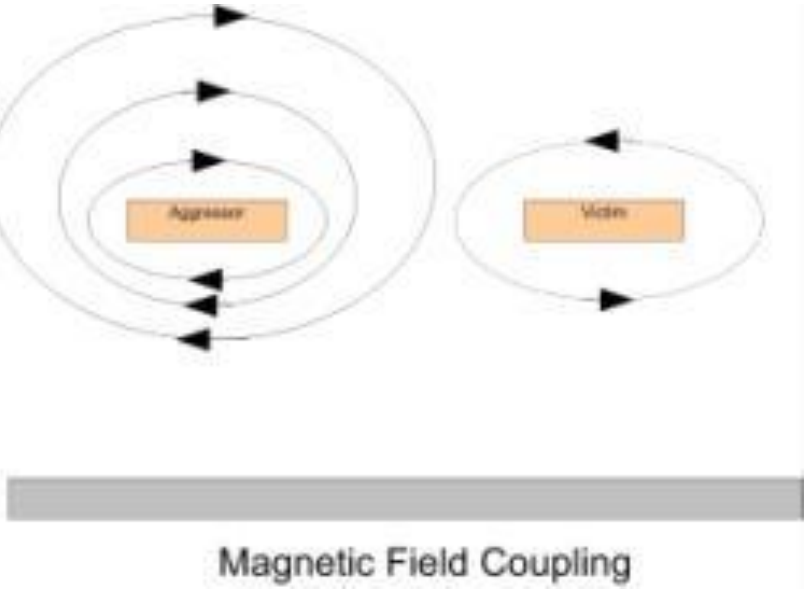
Capacitive Crosstalk: (Far End)

- Since the capacitively coupled current to the quiet line scales with dV/dt, the actual noise profile in the quiet line, moving to the far end, will be the derivative of the signal edge.
- If the signal edge is a linear ramp, the capacitively coupled-noise current will be a short rectangular pulse, lasting for a time equal to the rise time.
- The capacitively induced noise signature at the far end of the quiet line is illustrated below:
-



Inductive Crosstalk:

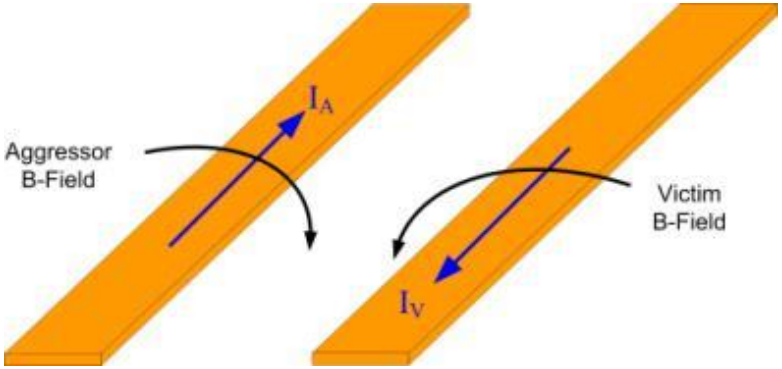
- Magnetic Fields exist as the current travels down the Aggressor line.
- These B-field lines induce B-field lines around the Victim line, which in turn creates current.
- The direction of the B-field lines in the Aggressor follow the Right-Hand-Rule.
- The direction of the B-field lines in the Victim are opposite of the Aggressor

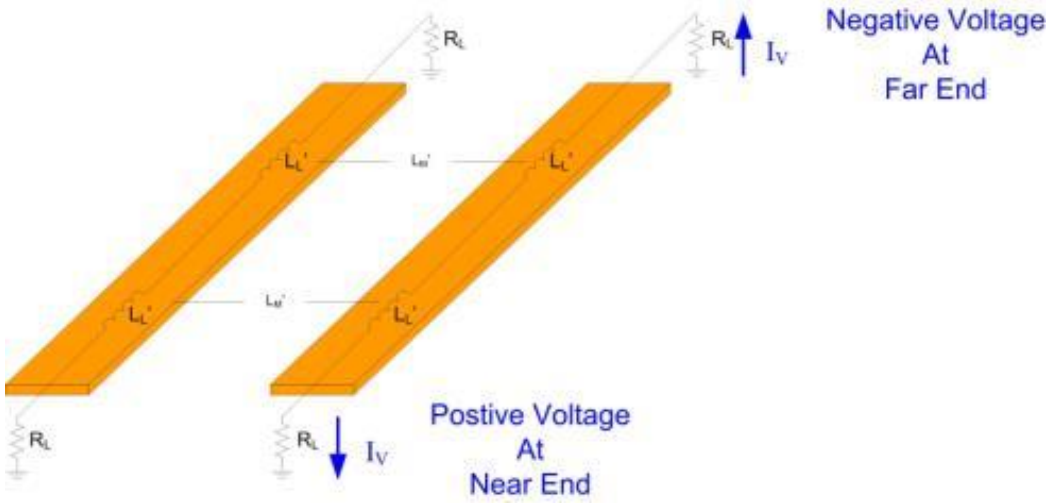


Magnetic Field Coupling

Inductive Crosstalk:

- The B-Field lines induced on the Victim create a current that flows in the opposite direction of the Aggressor current.
- The direction of the induced current creates a **Negative Voltage at the Far-End and a Positive Voltage at the Near-End** as it flows through the termination impedances.





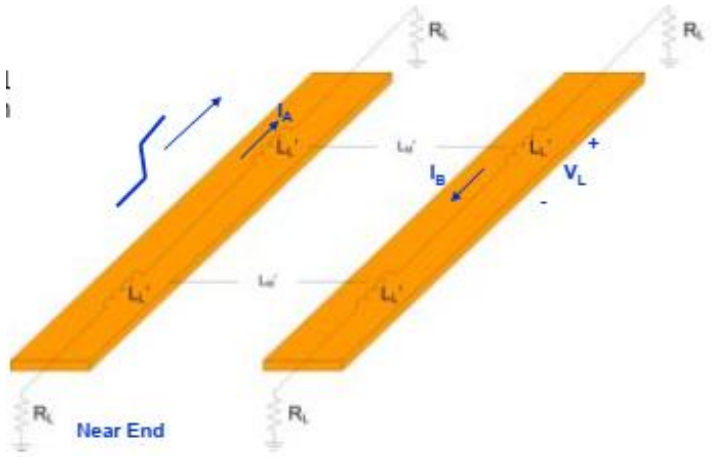
Inductive Crosstalk: (Near End)

- Just as in Near-End Capacitive crosstalk, the currents that are induced by the inductive coupling will travel back to the Source (or Near End) over a time span of 2·TD.
- The current that flows through the self inductance of the Aggressor line causes a voltage on the Victim line as follows:

$$V_M = L_M \cdot \frac{dI_A}{dt}$$

- This voltage appears across the Line inductance of the Victim which in turn causes a current to flow:

$$V_L = L_L \cdot \frac{dI_B}{dt}$$



Inductive Crosstalk: (Near End)

- Since the coupled voltage (VM) is the same as the Victim line voltage (VL) which creates the current, we can relate the currents of the Aggressor and Victim.

$$V_M = V_L$$

$$L_M \cdot \frac{dI_A}{dt} = L_L \cdot \frac{dI_B}{dt}$$

$$L_M \cdot \frac{I_A}{t_{rise}} = L_L \cdot \frac{I_B}{t_{rise}}$$

$$L_M \cdot \frac{I_A \cdot Z}{t_{rise}} = L_L \cdot \frac{I_B \cdot Z}{t_{rise}}$$

$$L_M \cdot \frac{V_A}{t_{rise}} = L_L \cdot \frac{V_B}{t_{rise}}$$

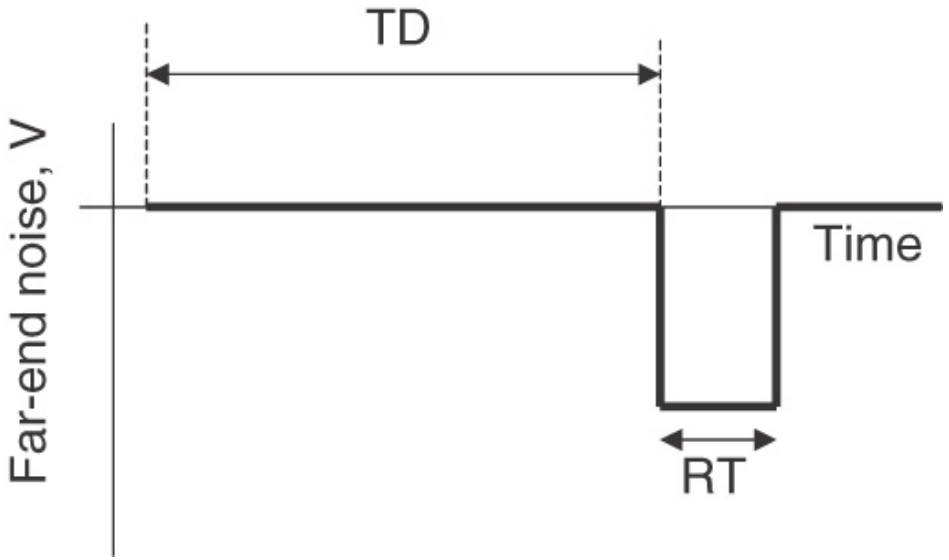
$$\frac{L_M}{L_L} = \frac{V_B}{V_A}$$

$$\left(\frac{V_{NE}}{V_A}\right)_{L_M} = \frac{1}{4} \cdot \left(\frac{L_M}{L_L}\right)$$

Inductive Crosstalk: (Far End)

- The exact derivation is applied to the Far-End inductive crosstalk to derive the maximum amount of noise due to Inductive coupling.
- The only difference is that the magnitude of the Far-End noise is **NEGATIVE**

$$\left(\frac{V_{FE}}{V_A}\right)_{L_M} = -\frac{1}{2}\cdot\left(\frac{length}{vel\cdot t_{rise}}\right)\cdot\left(\frac{L_M}{L_L}\right)$$



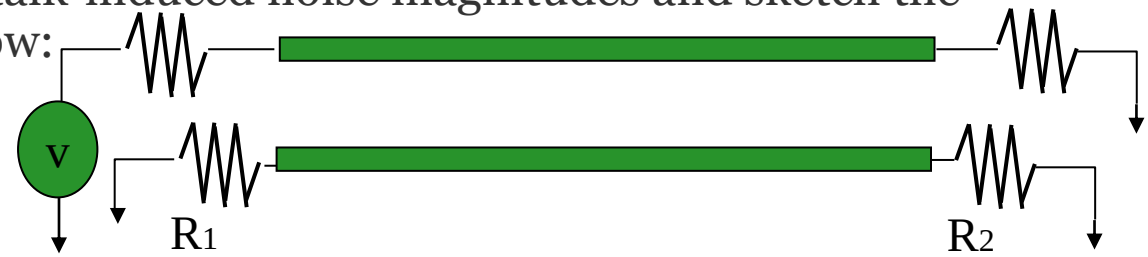
Crosstalk Equations Combination:-(Total X-talk)

$$NEXT = \left(\frac{V_{NE}}{V_A} \right) = \frac{1}{4} \cdot \left(\frac{C_M}{C_L} + \frac{L_M}{L_L} \right)$$

$$FEXT = \left(\frac{V_{FE}}{V_A} \right) = \frac{1}{2} \cdot \left(\frac{length}{vel \cdot t_{rise}} \right) \cdot \left(\frac{C_M}{C_L} - \frac{L_M}{L_L} \right)$$

Example:

Calculate near and far end crosstalk-induced noise magnitudes and sketch the waveforms of circuit shown below:



Vsource=2V, Trise = 100ps.
Length of line is 2 inches. Assume all terminations are 70 Ohms.
Assume the following capacitance and inductance matrix:

L / inch = $\begin{bmatrix} 9.869nH & 2.103nH \\ 2.103nH & 9.869nH \end{bmatrix}$

C / inch = $\begin{bmatrix} 2.051pF & 0.239pF \\ 0.239pF & 2.051pF \end{bmatrix}$

$$TD = d.\sqrt{LC}$$

$$\boldsymbol{Z_o = \sqrt{\frac{L_{11}}{C_{11}}}}$$

DECREASING FAR-END CROSS TALK:

1. Increase the spacing between the signal traces.
2. Decrease the coupling length.
3. Add dielectric material to the top of the surface traces.
4. Route the sensitive lines in stripline.

$$FEXT = \left(\frac{V_{FE}}{V_A} \right) = \frac{1}{2} \cdot \left(\frac{length}{vel \cdot t_{rise}} \right) \cdot \left(\frac{C_M}{C_L} - \frac{L_M}{L_L} \right)$$

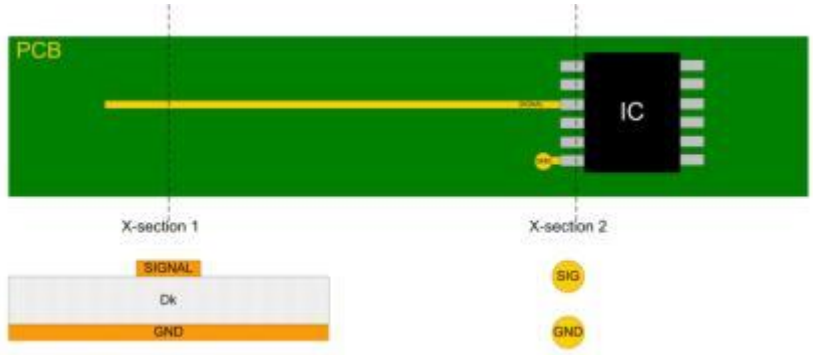
Switching Noise:

- When the **return path** is **highly inductive**, and the inductive noise dominates
  - When the inductance in **the return path** is the reason for the crosstalk
  - This is what we see on **packages** and in **connectors**
  - This is also called:

"Ground Bounce / Power Supply Droop"
"Simultaneous Switching Noise (SSN)"
"Simultaneous Switching Output (SSO) Noise"

Switching Noise:

- When **the return path is not a uniform plane**, the **inductive coupling** will **increase** much more than the **capacitive coupling**, and the noise will be dominated by the loop mutual inductance.
- This usually occurs in **small localized regions** of the interconnect, such as in **packages**, **connectors**, or **local regions** of the board where the return path is interrupted by gaps.
- When loop mutual inductance dominates, and it occurs in a small region, we can model the coupling with **a single lumped mutual inductor.**
- The noise generated in the quiet line by the mutual inductance arises only when there is **a dI/dt** in the active line, which is when the edge switches.
- For this reason, the noise created when mutual inductance dominates is sometimes called ***switching noise***, or ***dI/dt noise***, or ***delta I noise.***



Ground bounce:

- The return current that passes through the inductive interconnect causes a voltage to form following:

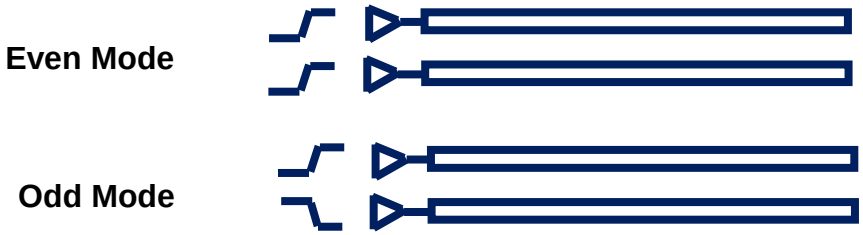
$$V_N = L_{ret} \cdot \frac{dI_A}{dt}$$

- This voltage changes the ground potential of the integrated circuit relative to the ground of the system which gives the name ***Ground Bounce***

Ground bounce is the voltage between two points in the return path due to a changing current in a loop. Ground bounce is the primary cause of switching noise and EMI. It is primarily related to the total inductance of the return path and shared return current paths. To decrease ground-bounce voltage noise, there are two significant features to change: Decrease the partial self-inductance of the return path by using short lengths and wide interconnects and increase the mutual inductance of the two legs by bringing the current and its return path closer together.

Odd and Even Mode Characteristics:

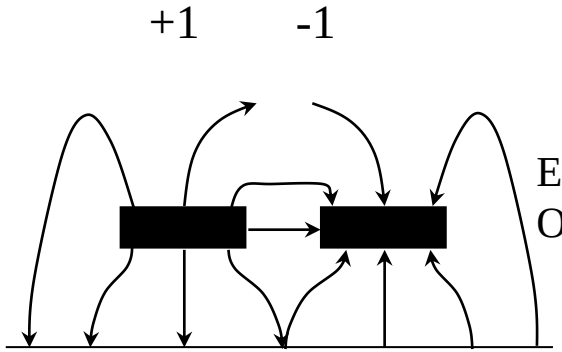
- *Electromagnetic Fields between two driven coupled lines will interact with each other.*
- *These interactions will affect the impedance and delay of the transmission line*
- *A 2-conductor system will have 2 propagation modes*
  - *Even Mode (Both lines driven in phase)*
  - *Odd Mode (Lines driven 180^{O} out of phase)*



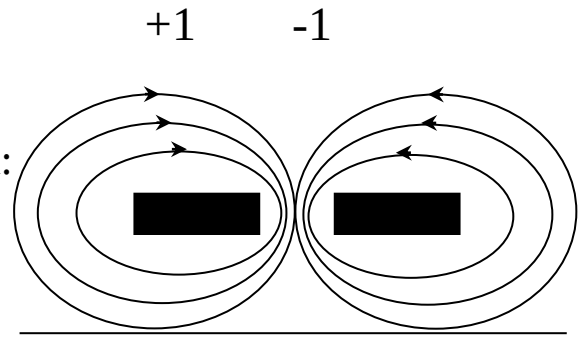
- *The interaction of the fields will cause the system electrical characteristics to be directly dependent on patterns*

Odd Mode Transmission

- Potential difference between the conductors lead to an *increase* of the effective Capacitance equal to the mutual capacitance

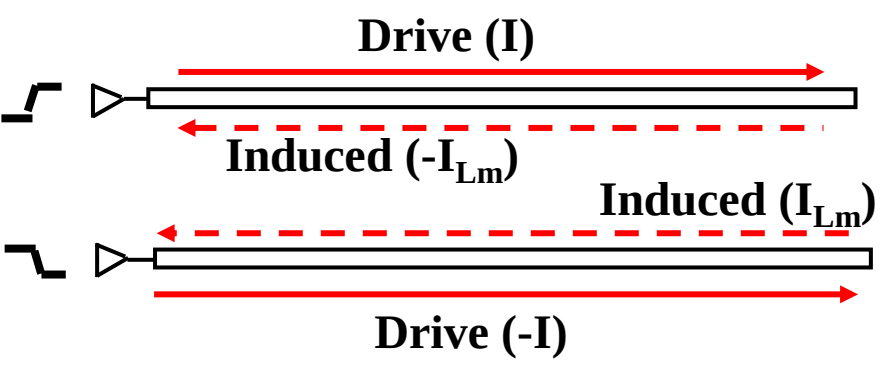


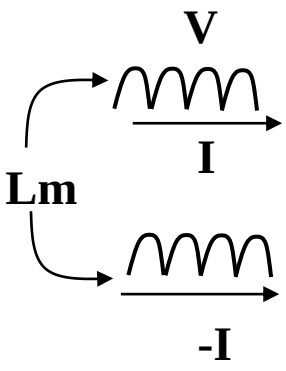
Electric Field:
Odd mode



Magnetic Field:
Odd mode

- Because currents are flowing in opposite directions, the total inductance is *reduced* by the mutual inductance (Lm)





$$V = L\frac{dI}{dt} + Lm\frac{d(-I)}{dt}$$

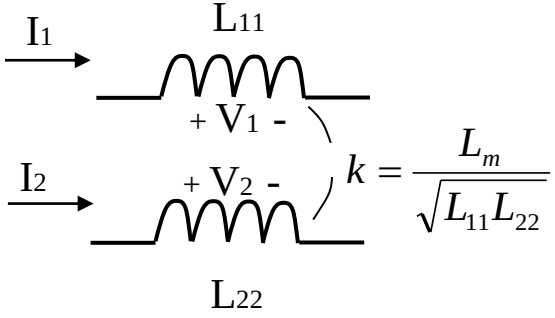
$$= (L - Lm)\frac{dI}{dt}$$

Odd Mode Transmission

"Derivation of Odd Mode Inductance"

Mutual Inductance:

Consider the circuit:



$$V_1 = L_O \frac{dI_1}{dt} + L_m \frac{dI_2}{dt}$$

$$V_2 = L_O \frac{dI_2}{dt} + L_m \frac{dI_1}{dt}$$

Since the signals for odd-mode switching are always opposite, $I_1 = -I_2$ and $V_1 = -V_2$, so that:

$$V_1 = L_O \frac{dI_1}{dt} + L_m \frac{d(-I_1)}{dt} = (L_O - L_m)\frac{dI_1}{dt}$$

$$V_2 = L_O \frac{dI_2}{dt} + L_m \frac{d(-I_2)}{dt} = (L_O - L_m)\frac{dI_2}{dt}$$

Thus, since $L_O = L_{11} = L_{22}$,

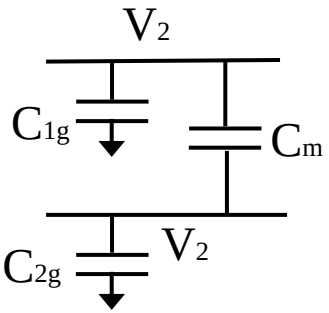
$$\boxed{L_{odd} = L_{11} - L_m = L_{11} - L_{12}}$$

Meaning that the equivalent inductance seen in an odd-mode environment is reduced by the mutual inductance.

Odd Mode Transmission: *"Derivation of Odd Mode Capacitance"*

Mutual Capacitance:

Consider the circuit:



$$C_{1g} = C_{2g} = C_O = C_{11} - C_{12}$$

So,

$$I_1 = C_O \frac{dV_1}{dt} + C_m \frac{d(V_1 - V_2)}{dt} = (C_O + C_m)\frac{dV_1}{dt} - C_m \frac{dV_2}{dt}$$

$$I_2 = C_O \frac{dV_2}{dt} + C_m \frac{d(V_2 - V_1)}{dt} = (C_O + C_m)\frac{dV_2}{dt} - C_m \frac{dV_1}{dt}$$

And again, $I_1 = -I_2$ and $V_1 = -V_2$, so that:

$$I_1 = C_O \frac{dV_1}{dt} + C_m \frac{d(V_1 - (-V_1))}{dt} = (C_{1g} + 2C_m)\frac{dV_1}{dt}$$

$$I_2 = C_O \frac{dV_2}{dt} + C_m \frac{d(V_2 - (-V_2))}{dt} = (C_O + 2C_m)\frac{dV_2}{dt}$$

Thus,

$$\boxed{C_{odd} = C_{1g} + 2C_m = C_{11} + C_m}$$

Meaning that the equivalent capacitance for odd mode switching increases.

Odd Mode Transmission

"Odd Mode Transmission Characteristics"

Impedance:

Thus, the impedance for odd mode behavior is:

$$Z_{odd} = \sqrt{\frac{L_{odd}}{C_{odd}}} = \sqrt{\frac{L_{11} - L_{12}}{C_{11} + C_{12}}}$$

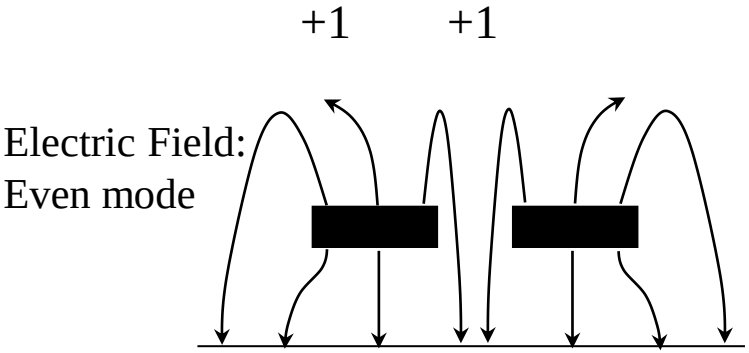
Propagation Delay:

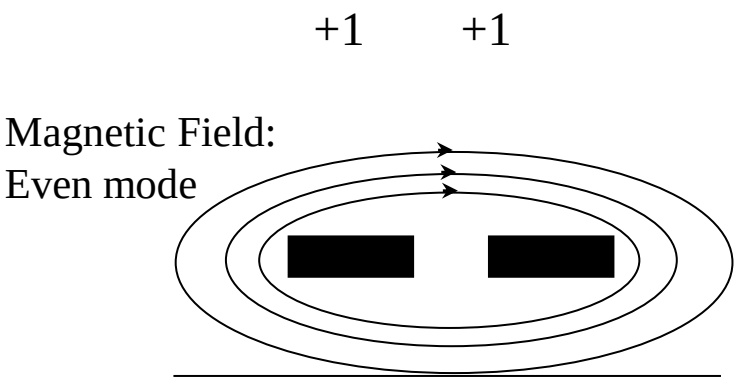
and the propagation delay for odd mode behavior is:

$$TD_{odd} = \sqrt{L_{odd} C_{odd}} = \sqrt{(L_{11} - L_{12})(C_{11} + C_{12})}$$

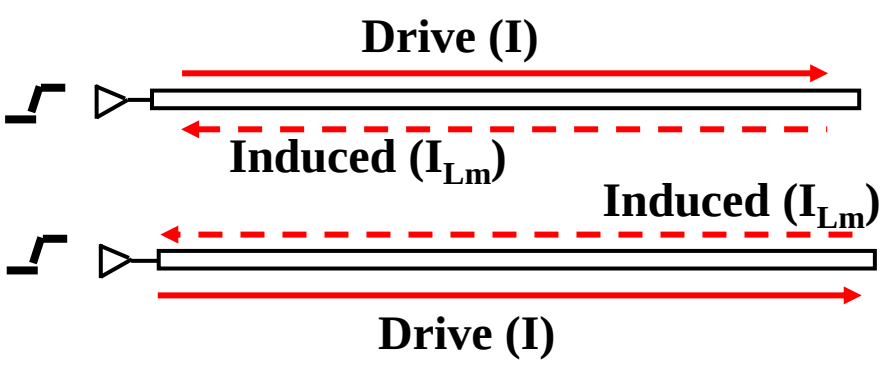
Even Mode Transmission

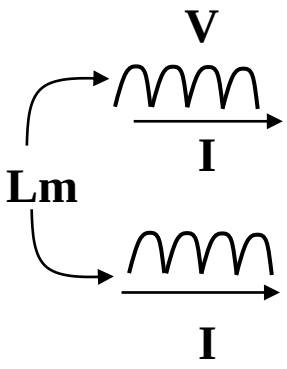
- Since the conductors are always at an equal potential, the effective capacitance is *reduced* by the mutual capacitance





- Because currents are flowing in the same direction, the total inductance is *increased* by the mutual inductance (Lm)





$$V = L\frac{dI}{dt} + Lm\frac{d(I)}{dt}$$

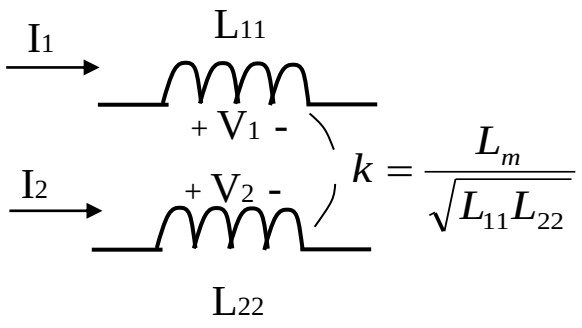
$$= (L + Lm)\frac{dI}{dt}$$

Even Mode Transmission

Derivation of even Mode Effective Inductance

Mutual Inductance:

Again, consider the circuit:



$$V_1 = L_O \frac{dI_1}{dt} + L_m \frac{dI_2}{dt}$$

$$V_2 = L_O \frac{dI_2}{dt} + L_m \frac{dI_1}{dt}$$

Since the signals for even-mode switching are always equal and in the same direction so that $I_1 = I_2$ and $V_1 = V_2$, so that:

$$V_1 = L_O \frac{dI_1}{dt} + L_m \frac{d(I_1)}{dt} = (L_O + L_m)\frac{dI_1}{dt}$$

$$V_2 = L_O \frac{dI_2}{dt} + L_m \frac{d(I_2)}{dt} = (L_O + L_m)\frac{dI_2}{dt}$$

Thus, $\boxed{L_{even} = L_{11} + L_m = L_{11} + L_{12}}$

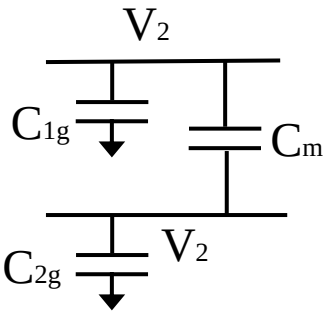
Meaning that the equivalent inductance of even mode behavior increases by the mutual inductance.

Even Mode Transmission

Derivation of even Mode Effective Capacitance

Mutual Capacitance:

Again, consider the circuit:



$$I_1 = C_O \frac{dV_1}{dt} + C_m \frac{d(V_1 - V_1)}{dt} = C_O \frac{dV_1}{dt}$$

$$I_2 = C_O \frac{dV_2}{dt} + C_m \frac{d(V_2 - V_2)}{dt} = C_O \frac{dV_2}{dt}$$

Thus, $\boxed{C_{even} = C_0 = C_{11} - C_m}$

Meaning that the equivalent capacitance during even mode behavior decreases.

Even Mode Transmission

"Even Mode Transmission Characteristics"

Impedance:

Thus, the impedance for even mode behavior is:

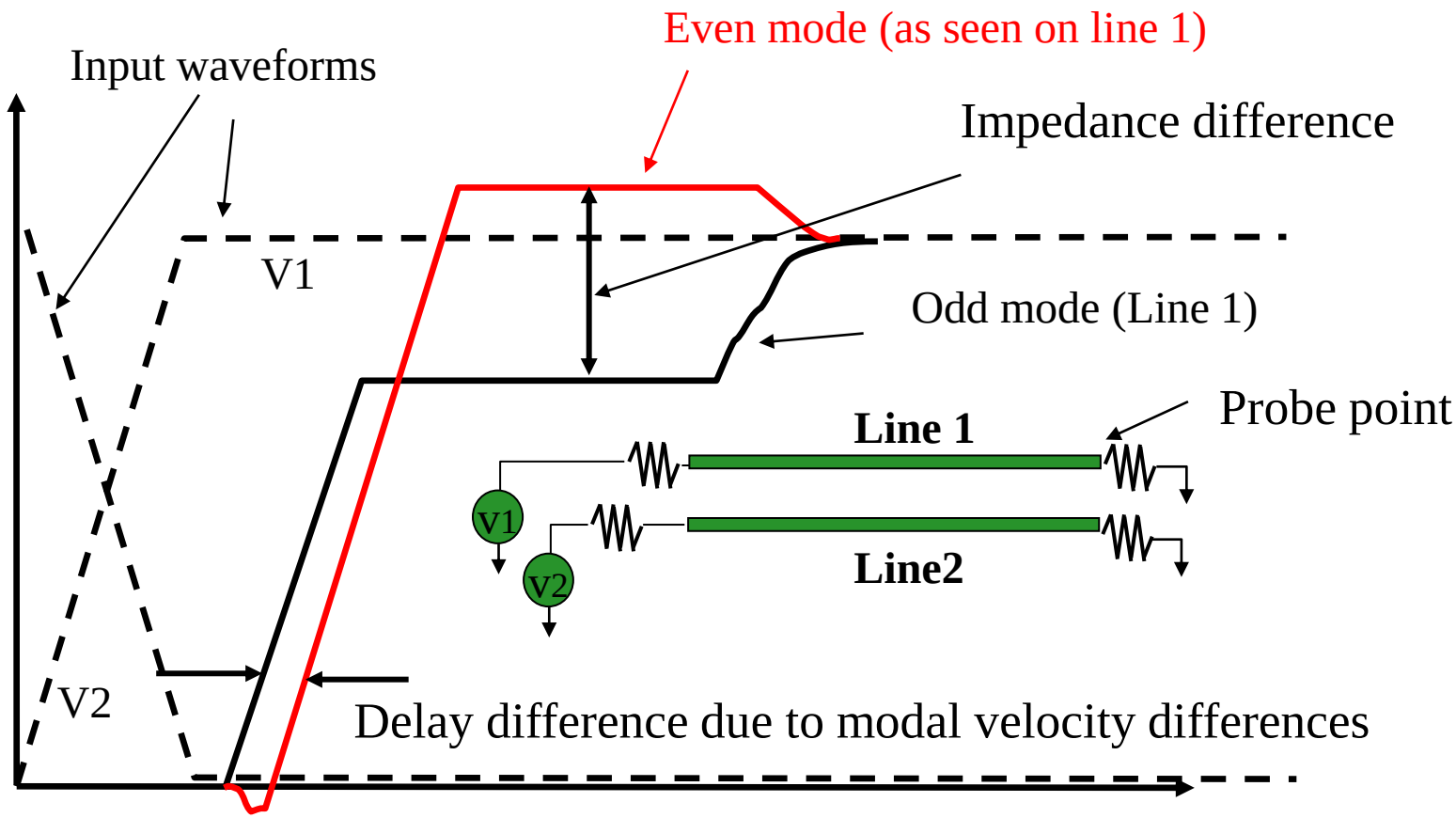
$$Z_{even} = \sqrt{\frac{L_{even}}{C_{even}}} = \sqrt{\frac{L_{11} + L_{12}}{C_{11} - C_{12}}}$$

Propagation Delay:

and the propagation delay for even mode behavior is:

$$TD_{even} = \sqrt{L_{even} C_{even}} = \sqrt{(L_{11} + L_{12})(C_{11} - C_{12})}$$

Odd and Even Mode Comparison for Coupled Microstrips



References

- **Signal and Power Integrity - Simplified by Eric Bogatin.**