

# Carbon Nanotubes for Data Processing

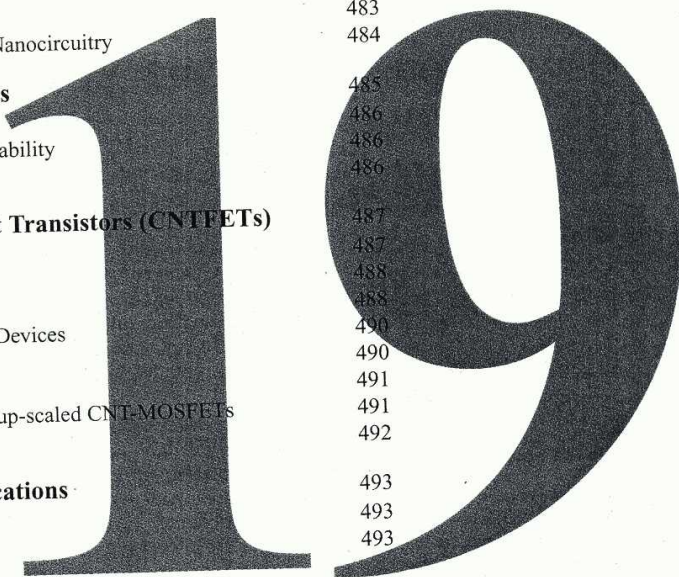
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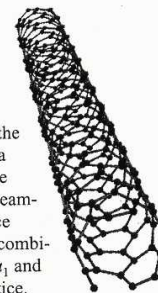
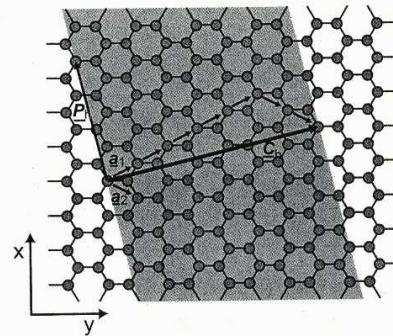
# Carbon Nanotubes for Data Processing

## 1 Introduction

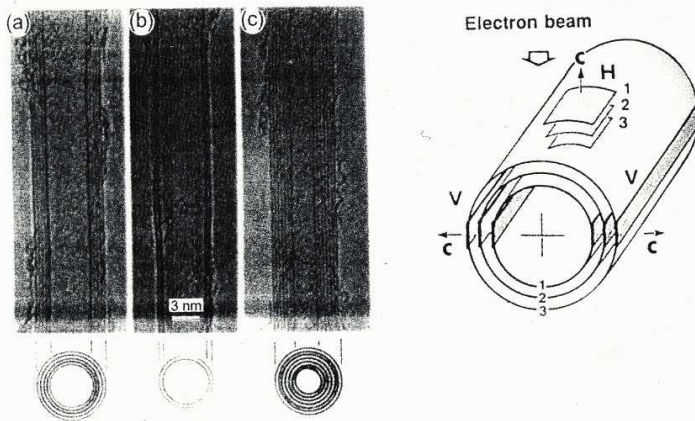
Carbon Nanotubes (CNTs) have been discovered by Sumio Iijima of the NEC Tsukuba laboratory in a HRTEM study of carbon filaments [1]. A CNT can be thought of as a stripe cut from a single graphite plane (so-called **graphene**) and rolled up to a hollow seamless cylinder (Figure 1). As in graphite, the C atoms form a hexagonal network. They are trigonally coordinated because of their  $sp^2$  hybridization. While in graphene, there is a pure  $sp^2$  hybridization, some small contributions of  $sp^3$  are mixed in, due to the curvature of the network in the case of CNTs.

With diameters between approx. 1 and 10 nm, the CNT cylinders can be tens of micrometers long. The ends may be open or capped with half a fullerene molecule in case of highly symmetrical nanotubes. Besides single-wall nanotubes (SWNT), there are multi-wall nanotubes (MWNT) which consist of numerous cylinders tightly stuck into another (Figure 2). In addition, ropes of CNTs are frequently encountered. These ropes are self-assembled bundles of (typically single-wall) nanotubes, in which the tubes line-up parallel to each other (Figure 3).

For electronic applications on the basis of carbon nanotubes or any other novel material the question to address is: "How can CNTs be employed in microelectronic and nanoelectronic devices?" The existing silicon based technology is extremely successful in producing the basic elements of integrated circuits, transistors and interconnects, at ever smaller dimensions in a highly parallel and cost effective process. Thus, a new technology, that wants to compete with a mature and reliable mainstream approach has to offer significant benefits. On the other hand, the constant scaling of length dimensions,



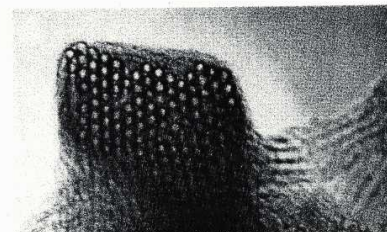
**Figure 1:** Arrangement of the C atoms in graphene with a roll-up stripe (grey) and the resulting nanotube. For a seamless tube, the circumference vector  $C_h$  must be a linear combination of the unit vectors  $a_1$  and  $a_2$  of the 2-D graphene lattice.



**Figure 2:** TEM image and imaging scheme of multi-wall nanotubes with various inner and outer diameters,  $d_1$  and  $d_0$ , and numbers of cylindrical shells  $N$  reported by Iijima [1]:  
 (a)  $N = 5$ ,  $d_0 = 6.7$  nm,  
 (b)  $N = 2$ ,  $d_0 = 5.5$  nm,  
 (c)  $N = 7$ ,  $d_1 = 2.3$  nm,  $d_0 = 6.5$  nm.

which is the driving force behind the continuously improving silicon technology, will unavoidably lead to molecular and even atomic dimensions, where the toolkit developed for processing in the  $\mu\text{m}$ -range will eventually cease to be the optimum choice. The small size (diameter) of nanotubes in combination with their transport properties are very attractive in this context. CNT technology offers a new approach that may turn out to be more suitable for devices with nanometer-scale dimensions.

This Chapter will mainly focus on SWNTs although MWNT will be described too. It will describe the structure, the electronic properties, the synthesis, and first device concepts which have been published in recent years. We will restrict the discussion in this Chapter to nanoelectronics device applications although there are other interesting applications of nanotubes such as field emission displays, light sources, actuators, sensors and batteries. For a more comprehensive and more general coverage of CNT topic see, for example: Refs. [2], [3].



**Figure 3:** TEM cross section of a rope of SWNTs illustrating a hexagonal (i. e. densely packed) arrangement of the aligned tubes [4], [5].

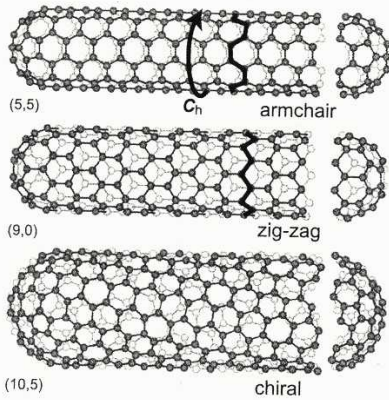


Figure 4: Examples of CNTs with different circumference vectors  $C_h$  [5].

## 2 Electronic Properties

### 2.1 Geometrical Structure

The structure of CNTs is described by the circumference vector or **chiral vector**  $C_h$ , which represents the full circumference of the tube. It is defined by

$$C_h = na_1 + ma_2 \tag{1}$$

where  $a_1$  and  $a_2$  are the unit vectors in the hexagonal lattice, and  $n$  and  $m$  are integers (Figure 1).  $C_h$  also defines the propagation vector  $P_h$  representing the periodicity of the tube parallel to the tube axis. Furthermore, it settles the so-called chiral angle which is the angle between  $C_h$  and  $a_1$ . If either  $n$  or  $m$  are zero, the chiral angle is  $0^\circ$  and the structure is called *zig-zag*. If  $n = m$ , the chiral angle is  $30^\circ$  and the structure is called *arm-chair* (Figure 4). All other nanotubes show chiral angles between  $0^\circ$  and  $30^\circ$ . They are known as *chiral* nanotubes because they produce a mirror image of their structure upon an exchange of  $n$  and  $m$ .

Experimentally, the diameter of nanotubes is frequently determined by TEM, STM or AFM. The chiral structure can be determined by STM (Figure 5).

### 2.2 Electronic Structure of Graphene

For the discussion of the electronic structure of CNTs, we start again with graphene. As an extension of the description of fused benzene (Chap. 5), in graphene, a bonding  $\pi$ -band and an anti-bonding  $\pi^*$ -band is formed from the overlap between  $2p_z$ -AOs of adjacent atoms. P. R. Wallace [7] derived an expression for the 2-D energy states,  $W_{2D}$ , of the  $\pi$ -electrons in the graphene plane as a function of the wave vectors  $k_x$  and  $k_y$  (see also [8]):

$$W_{2D}(k_x, k_y) = \pm \gamma_0 \left[ 1 + 4 \cos\left(\frac{\sqrt{3}k_x a}{2}\right) \cos\left(\frac{k_y a}{2}\right) + 4 \cos^2\left(\frac{k_y a}{2}\right) \right]^{1/2} \tag{2}$$

where  $\gamma_0$  denotes the nearest-neighbour overlap (or: transfer) integral and  $a = 0.246 \text{ nm}$  is the in-plane lattice constant. The two different signs in Eq. (2) represent the  $\pi$ - and  $\pi^*$ -band. The calculations show that the  $\pi$ - and  $\pi^*$ -band just touch each other at the corners of the 2-D Brillouin zone (Figure 6). In the vicinity of the  $\Gamma$  point, the dispersion relation is parabolically shaped, while towards the corners (K points) it shows a linear  $W(k)$  dependence. At  $T = 0 \text{ K}$ , the  $\pi$ -band is completely filled with electrons and the  $\pi^*$ -band is empty. Because the bands only touch at the K points, integration over the Fermi surface (which is a line for a two-dimensional system) results in a vanishing density of states. On the other hand no energy gap exists in the graphene dispersion relation. This means we are dealing with the unusual situation of a gapless semiconductor. (The real graphite yet is a metal since the bands overlap by approx. 40 meV due to the interaction of the graphene planes.)

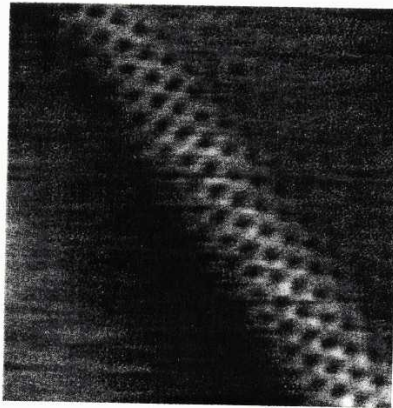


Figure 5: STM image at 77 K of a SWNT at the surface of a rope [6].

### 2.3 Electronic Structure of Carbon Nanotubes

For the description of the band structure of graphene, it has been assumed that the graphene plane is infinite in two dimensions. For CNTs, we have a structure which is macroscopic along the tube axis, but the circumference is in atomic dimensions. Hence, while the density of allowed quantum mechanical states in axial direction will be high, the number of states in the circumferential direction will be very limited. More precisely, the roll-up by the chiral vector  $C_h$  leads to periodic boundary conditions in the circumferential direction. Quantum mechanically, these boundary conditions define allowed modes (1-D states) along the tube axis according to:

$$C_h \cdot k = 2\pi j \quad \text{with } |j| = 0, 1, 2, \dots \tag{3}$$

In the case of arm-chair tubes, the periodic boundary condition yield allowed values for the wave vector in circumferential direction according to:

$$k_{y,j} = \frac{j}{q_y} \frac{2\pi}{\sqrt{3}a} \tag{4}$$

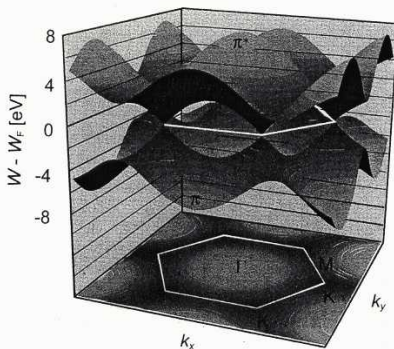
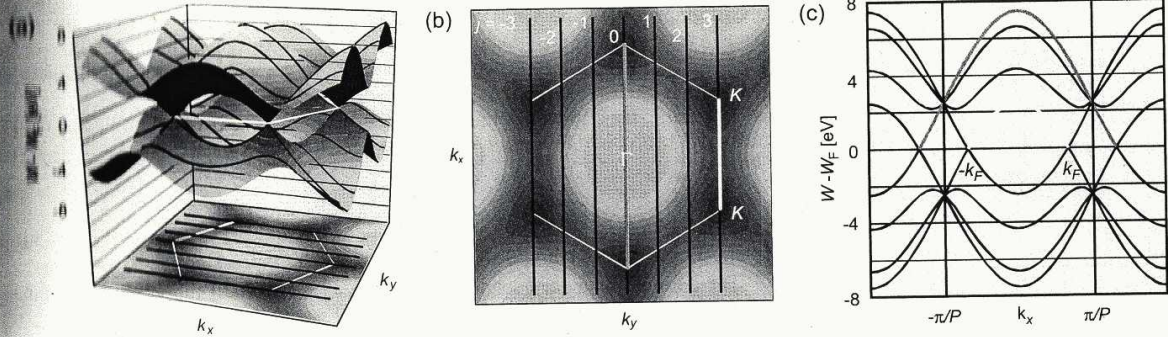
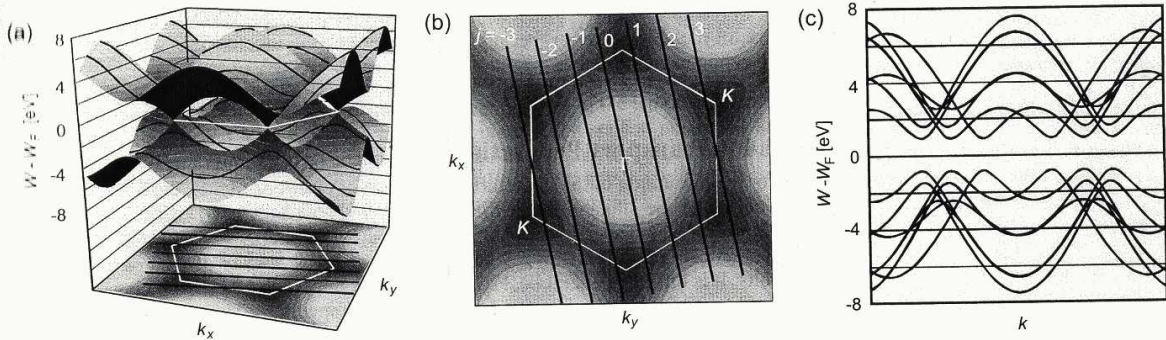


Figure 6: 3-D illustration of the dispersion relation of graphene.



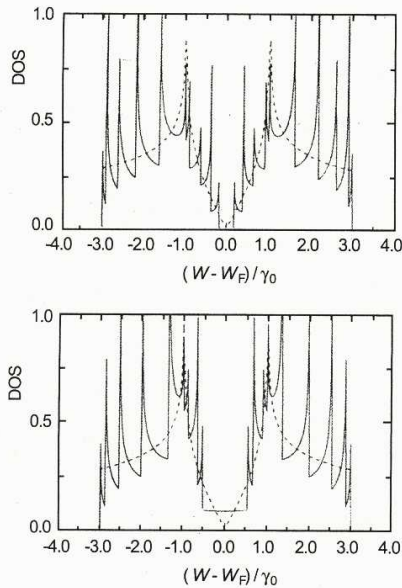
**Figure 7:** Dispersion relation of a (3,3) CNT. (a) 3-D illustration of the dispersion relation for graphene including the allowed states for the (3,3) CNT. The periodic boundary conditions along the circumference of the tube result in a discrete set of allowed  $k_y$  values. (b) Projection of the allowed states onto the first Brillouin zone of graphene. Obviously, the K points are allowed states for CNTs of this chirality. (c) 2-D illustration of the dispersion  $W(k_x)$ . The states at the Fermi level indicate the metallic behaviour of this tube. The periodicity volume in the  $k$  space is given by the interval from  $-\pi/P$  to  $+\pi/P$ .

**Figure 8:** Dispersion relation of a (4,2) CNT. (a) 3-D illustration of the dispersion relation for graphene including the allowed states for the (4,2) CNT. The periodic boundary conditions along the circumference of the tube result in a discrete set of allowed  $k$  values. (b) Projection of the allowed states onto the first Brillouin zone of graphene. Obviously, the K points are no allowed states for CNTs of this chirality. (c) 2-D illustration of the dispersion  $W(k)$ , the conduction band and the valence band are separated by a bandgap.



where  $q_y = n = m$ . For the armchair geometry, the tube axis is identical to the  $x$ -direction and the circumference represents the  $y$ -direction. As an example of an armchair tube, Figure 7 shows the dispersion relation, the projection of the allowed 1-D states onto the first Brillouin zone of graphene, as well as the  $W(k_x)$  relation for a (3,3) tube. Due to the periodic boundary conditions, i. e. by inserting Eq. (4) into Eq. (2), the allowed states condense into lines (black lines in Figure 7a). Here, there are  $q_y = 3$  lines on either side of the center of the Brillouin zone and an additional line going through the center. In case of a (3,3) tube the allowed states include the K points. Since the system is now one-dimensional in an electronic sense, different from the case of graphene, the integration over the Fermi surface (which is the sum over the Fermi points) yields a finite density of states at the Fermi energy. The (3,3) tube, and armchair tubes in general, show a *metallic* behavior.

As an example of a chiral tube, Figure 8 shows the dispersion relation, the projection of the allowed 1-D states onto the first Brillouin zone of graphene, as well as the  $W(k_x)$  relation for a (4,2) tube. We will illustrate why the electronic properties of this (4,2) tube is very different from the (3,3) tube despite their very similar diameters. Again, due to the periodic boundary conditions, the allowed states condense into lines (black lines in Figure 8a). In contrast to the (3,3) tube, the  $C_h$  vector is not parallel to the  $y$ -direction and, hence, leads to a mixed quantization of  $k_x$  and  $k_y$ . The propagation of an electron along the tube axis is described by a combination of  $k_x$ - and  $k_y$ -components. For this reason, the general letter  $k$  is used in Figure 8c, representing the momentum of the electron in the direction of propagation. The band structure of (4,2) tubes is deter-



**Figure 9:** Calculated density of states (DOS) per unit cell of graphene as a function of energy,  $W$ , normalized by the overlap integral  $\gamma_0$  [9].  
 (a) Result for a (10,0) tube, showing a bandgap around  $W_F$ .  
 (b) Result for a (9,0) tube, showing no bandgap. For comparison, the dashed lines represent the DOS for graphene.

mined by the fact that there are no modes which include the K points of the Brillouin zone of graphene (Figure 8b). The Fermi level is not dependent on the  $C_h$  vector,  $W_F$  is now in a bandgap, i. e. this type of tube is a *semiconductor*. The bandgap is of the order of a few eV (Figure 8c). In general, the bandgap decreases with increasing diameter of the tube.

In general, the semiconducting or metallic behavior of CNTs is controlled by the  $C_h$  vector and, hence, by the relation of  $n$  and  $m$ . Metallic behavior occurs for

$$n - m = 3q \quad (5)$$

where  $q$  is an integer. As a consequence, one-third of all CNTs types are metallic for a statistic distribution of chiralities including all armchair types, since  $q = 0$  for them.

The periodic boundary conditions for zig-zag tubes,  $(n,0)$  tubes and  $(0,m)$  tubes, results in allowed wave vectors according to

$$k_{x,j} = \frac{j}{q_x} \frac{2\pi}{a} \quad (6)$$

The condition for metallic tubes, Eq. (5), is fulfilled for one-third of the tubes, i. e. if  $n$  or  $m$  are multiples of three. Figure 9 illustrates the density of state (DOS) for two zig-zag type CNTs [9], a (10,0) tube showing a bandgap and, hence, semiconducting behavior (Figure 9a), and a (9,0) tube showing no bandgap and, hence, metallic behavior (Figure 9b).

The discussion so far has been restricted to isolated SWNTs. Theoretical and experimental studies have shown that the intertube coupling within MWNTs and ropes of SWNTs [10], [11] have a relatively small effect on the band structure of a tube [12]. As a consequence, semiconducting and metallic tubes retain their character if they are a part of MWNTs or ropes. By statistical probability, most of the MWNTs and ropes show an overall metallic behavior, because one single metallic tube is sufficient to short-circuit all semiconducting tubes.

## 2.4 Transport Properties

For the discussion of the unperturbed transport of electrons in metallic SWNTs, we consider again the situation near the Fermi level shown by the 1-D dispersion spectrum, Figure 7c. The dispersion relation around the Fermi energy is linear. Furthermore, the energetical separation,  $\Delta W_{\text{mod}}$  between the modes at  $\pm k_F$  is of the order of electron volts. It is this large energetical spacing between the 1-D subbands which prevents interband scattering to a large extent even at room-temperature. The transport is constrained to a single 1-D mode. Since there are subbands with positive and negative slope at both,  $+k_F$  as well as for  $-k_F$ , one expects a Landauer conductance

$$G = 2 \cdot 2 \cdot \frac{e^2}{h} = \frac{4e^2}{h} \quad (7)$$

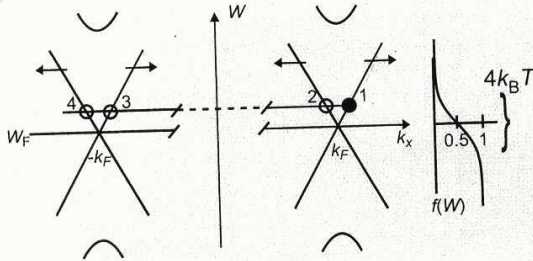
for an ideal, scattering-free i. e. **ballistic transport** of a metallic CNT. The degeneracy due to the spin is considered by a factor 2.

According to different authors (e.g. [50]) it is expected that ballistic transport properties are maintained in carbon nanotubes over distances of several micrometers. For transport on a larger scale scattering has to be taken into account.

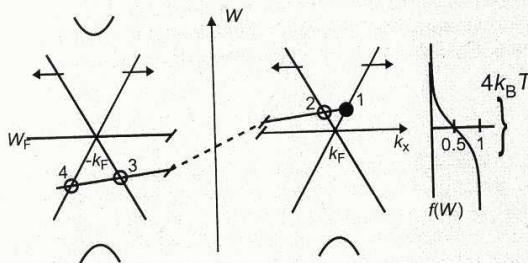
We will first consider the elastic **scattering at impurities**. For 3-D metals, the probability of a scattering event, i. e. the scattering rate, is described by the classical Rutherford scattering theory:

$$\tau_{\text{imp}}^{-1} \propto v_F \cdot \frac{1}{v_F^4} = v_F^{-3} \quad (8)$$

where  $v_F$  denotes the Fermi velocity. In particular,  $\tau_{\text{imp}}^{-1}$  is independent of temperature. This result relies on the fact that the velocity of electrons in an interval of approx.  $4 k_B T$  around the Fermi energy is given by  $v_F$  in a very good approximation. This is in general a valid assumption for 3-D metals where  $W_F$  is large compared to  $k_B T$ . Eq. (8) holds exactly, if the dispersion relation is linear within the energy interval of approx.  $4 k_B T$ . This condition is fulfilled for CNTs up to room temperature and above. Figure 10 is a magnification of Figure 7c and shows the segment of the dispersion relation in the vicinity of the Fermi positions at  $\pm k_F$ . The arrows indicate the Fermi velocities of the elec-



**Figure 10:** Illustration of impurity scattering processes on a metallic CNT. Dispersion relation in the vicinity of  $-k_F$  and  $+k_F$  as well as the Fermi-Dirac occupancy relation are shown. Position 1 (black circle) indicates an initial state of an electron, the positions 2 to 4 are potential final states after scattering events.



**Figure 11:** Illustration of an acoustic phonon scattering event on a metallic CNT. Dispersion relation in the vicinity of  $+k_F$  as well as the Fermi-Dirac occupancy relation are shown. Position 1 (black circle) indicates an initial state of an electron, position 2 is the final state after the scattering event.

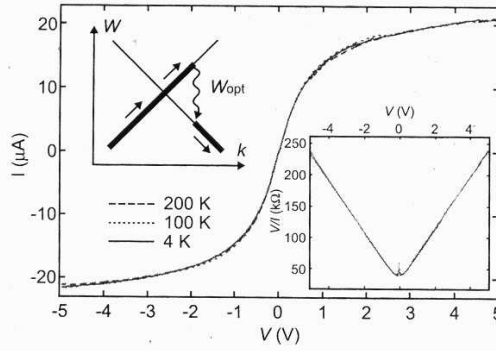
trons. Scattering at an impurity is an elastic scattering process. Consequently, an electron can only be scattered in another state at the *same* energy of the nanotube dispersion relation. The allowed final states for an electron in an initial state at position 1 are indicated as 2 to 4 in Figure 10. The change in electron momentum is accounted for by the impurities. Because of the one-dimensionality of the system, small-angle scattering as present in 2-D or 3-D metals does not exist in carbon nanotubes. While scattering from 1 to 3 represents a forward scattering event without effect on the sample conductance, scattering from 1 to 2 or 4 is a backscattering event and will increase the CNT resistance. The two-terminal resistance of a CNT segment of length  $L$  will be

$$R_{\text{imp}} = \frac{h}{4e^2} \cdot \frac{L}{\lambda_{\text{imp}}} \quad (9)$$

where  $\lambda_{\text{imp}}$  is the elastic mean free path which is roughly speaking the average distance between impurity centers.  $R_{\text{imp}}$  will be temperature independent in a good approximation.

For the discussion of the **phonon scattering** of electrons on CNTs, we have to distinguish scattering by optical and acoustical phonons. Starting point for describing the latter is the linear dispersion of the *acoustical phonons* with  $W_{\text{ph}} = \hbar c_{\text{ph}} k_{\text{ph}}$  [13]. Since the velocity of sound,  $c_{\text{ph}}$ , is approx.  $10^4$  m/s, i.e. about two orders of magnitude smaller than the Fermi velocity of the electrons ( $v_F \cong 10^6$  m/s), the scattering of an electron by an acoustic phonon results in a rather small electron energy change. Figure 11 illustrates a possible final state 2 for an electron scattered by an acoustic phonon from an initial state 1. The two states are connected through a line with a slope ( $c_{\text{ph}}$ ) much smaller than the one of the electron dispersion relation reflecting the aforementioned difference in velocities. Scattering from the crossed dispersion region around  $+k_F$  to  $-k_F$  is suppressed because there are no empty, allowed states available around  $-k_F$  even at room-temperature. This can be understood as follows: Scattering from  $+k_F$  to  $-k_F$  requires a  $\Delta k$  of approximately  $2k_F$  which has to be delivered by the phonon. This means  $k_{\text{ph}} = \Delta k = 2k_F$ . The corresponding phonon energy is  $W_{\text{ph}} = \hbar c_{\text{ph}} k_{\text{ph}} \cong 100$  meV. This value is much higher than  $k_B T$  even at room-temperature and thus scattering from around  $+k_F$  to  $-k_F$  is suppressed. On the other hand, scattering from 1 to 2 remains possible even at lowest temperatures. This is true because the required energy transfer  $W_{\text{ph}}$  is always smaller than the electrical excess energy of the electron in position 1, since  $c_{\text{ph}} \ll v_F$ .

**Figure 12:** High-field  $I$ - $V$  characteristics for metallic CNTs at different temperatures. The right inset plots  $V/I = R$  vs.  $V$ . The left inset shows a section of the dispersion relation and illustrates the phonon emission [14].



A quantitative expression for the temperature dependence of the acoustical phonon scattering can be derived from a consideration of the dimensions. Since the Debye temperature of CNT is approx. 2000 K [14], the situation for  $T < 300$  K is described by the Grüneisen relation. For 3-D metals, this is a dependence of the scattering rate according to

$$\tau_{ph}^{-1} \propto T^5 \tag{10}$$

This temperature dependence is composed of three factors. A first  $\propto T^2$  dependence results from the density of phonon states in three dimensions. A second  $\propto T^2$  term describes the small-angle scattering in 3-D metals. And finally, there is factor  $\propto T$  from the energy transfer between electron and phonon. For 1-D systems such as CNTs, the first two terms have to be changed to  $\propto T^0$ , because the 1-D phonon DOS shows no temperature dependence and the small-angle scattering is not allowed in 1-D structures. The final  $\propto T$  term remains and, hence, the resistance contribution due to acoustical phonon is given by

$$R_{ph} = \frac{h}{4e^2} \cdot \frac{L}{\lambda_{ph}} \text{ where } \lambda_{ph} = v_F \cdot \tau_{ph} \text{ and } \tau_{ph} \propto T^{-1} \tag{11}$$

For small electric excess energies of the electrons (approx.  $eV < 100$  meV), scattering by optical phonons can be neglected since there are no unoccupied states at energies

$$W_{final} = W_{initial} - W_{opt} \tag{12}$$

where  $W_{opt}$  denotes the energy of optical phonons [14]. For large dc biases, i. e. high fields, electrons on the CNT are taking up energies well beyond values of  $k_B T$ ; they become *hot*. Interestingly, hot in this case does not mean that the electron velocity has increased. Because of the special situation of a linear dispersion relation, the velocity of the carriers remains constant while their energy increases. This changes the situation completely. In the case of hot electrons, scattering by optical phonons can be the main contribution to the overall resistance of CNTs. Figure 12 shows the high-field  $I$ - $V$  characteristics of metallic CNTs at different temperatures. The curves overlap almost completely, proving a temperature independent behavior. For small voltages, approx.  $V = 0.2$  V, the  $I$ - $V$  characteristics exhibits a linear behavior. For larger voltages, the  $I$ - $V$  curve is strongly non-linear. For voltages approx.  $> 5$  V, the current exceeds  $20 \mu A$  which corresponds to a current density of more than  $10^9$  A/cm<sup>2</sup>. Furthermore, it seems that a saturation current  $I_0$  is approached at large bias. The resistance shows a constant value  $R_0$  at small bias and increases linearly for  $V > 0.2$  V (see right inset in Figure 12), i.e. it can be expressed by:

$$R = R_0 + V/I_0 \tag{13}$$

This behaviour can be explained by the inset picture in the left of Figure 12. Once an electron has gained enough energy to emit an optical phonon, it is immediately backscattered [15]. A steady state is approached in which the electrons moving in forward direction have an energy  $W_{opt}$  higher than the backward moving ones. This leads to a saturation current

$$I_0 = \frac{4e^2}{h} \cdot \frac{W_{opt}}{e} \tag{14}$$

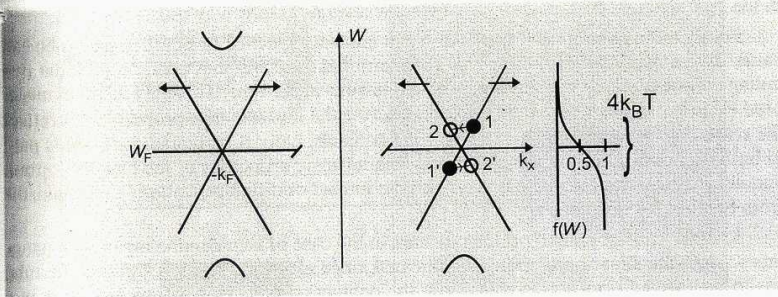


Figure 13: Illustration of an electron-electron scattering event on a metallic CNT. Dispersion relation in the vicinity of  $+k_F$  as well as the Fermi-Dirac occupancy relation are shown. Positions 1 and 1' (black circles) indicate the initial state of the two electrons, positions 2 and 2' are the final states after the scattering event.

Here, the first term on the right represents the Landauer conductance as before and the second the voltage corresponding to  $W_{opt}$ . Using a value of approx. 160 meV [14], Eq. (14) leads to a saturation current of approx. 25 mA, in very good agreement with the experimental results. Accordingly, the mean free path  $l_{opt}$  for backscattering phonons is just the distance an electron needs to accumulate the threshold energy:

$$\lambda_{opt} = \frac{W_{opt}}{e} \cdot \frac{L}{V} \quad (15)$$

$L$  denotes the electrode spacing and  $V$  the applied voltage, i.e.  $V/L$  is the electric field along the CNT. If this is combined with a field-independent scattering term (i. e. from impurities) with a mean free path  $\lambda_{imp}$ , an overall expression for the voltage dependent resistance can be obtained:

$$R = \frac{h}{4e^2} \cdot L \left( \frac{1}{\lambda_{imp}} + \frac{1}{\lambda_{opt}} \right) = \frac{hL}{4e^2 \lambda_{imp}} + \frac{h}{4eW_{opt}} \cdot V \quad (16)$$

The right equation is obtained by inserting Eq. (15) into the expression for  $\lambda_{opt}$ , Eq. (16) fully explains the empirical result, Eq. (13).

An additional mechanism that leads to a resistance contribution is the **electron-electron scattering**; a mechanism which may get especially pronounced in 1-D conductors. Typically, electron-electron scattering does not result in any measurable change in resistance for a normal conductor. This is true because energy and momentum conservation can only be fulfilled if as many electrons are backscattered as get scattered in the forward direction. The situation is drastically changed for a carbon nanotube. Figure 13 shows the dispersion relation in the vicinity of  $k_F$ . Because of the mode crossing, two electrons in the positions 1 and 1', which contribute to the forward transport, may get scattered in positions 2 and 2', respectively. The total energy and momentum is conserved during this process. The scattered electrons in 2 and 2' now occupy states in the negative current direction. Hence, this process leads to a resistance increase. With raising temperature, the number of allowed initial and final states increases and so does the scattering probability. A detailed analysis [16] reveals a linear dependence of the electron-electron scattering rate on the temperature:

$$R_{e-e} = \frac{h}{4e^2} \cdot \frac{L}{\lambda_{e-e}} \quad \text{with} \quad \tau_{e-e} \propto T^{-1} \quad (17)$$

where  $\lambda_{e-e}$  is the mean free path between scattering events and  $\tau_{e-e}$  is the inverse scattering rate. The scattering rate also rises with increasing electric excess energies,  $eV$ , of the electrons because the number of allowed states increases.

## 2.5 Contacts

In order to perform any kind of electrical measurement on a carbon nanotube it is essential to create some kind of contact between the tube and the outside world. One way of doing this is to localize the position of a tube, or a rope of tubes by means of a scanning electron microscope (SEM) and then design the desired contact geometry by electron beam lithography, metal deposition and lift-off. A typical example of such a structure is shown in Figure 14.

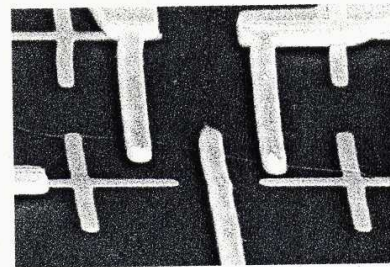


Figure 14: SEM image of a rope of single-wall nanotubes contacted by several gold fingers attached to the top of the tube.



As with any other system, a highly transmissive, minimum invasive contact is important to study the tube properties. But exactly this type of contact is hard to achieve in the context of carbon nanotubes. There are several reasons why this is the case.

For metallic nanotubes it was found that contacts attached to a carbon nanotube can cause severe backscattering. E.g. in a four-terminal measurement configuration the two voltage probes can significantly influence transport in the tube. This may result in measured electrical characteristics that do not describe the intrinsic tube properties but reflect the scattering situation in the vicinity of the contacts. Only if particular attention is paid to buffer the impact of the metal contacts, the intrinsic properties of the metallic carbon nanotube can be studied and the theory on the impact of different scattering mechanisms from Section 2.4 becomes applicable [17].

Another contact related problem occurs in the case of semiconducting carbon nanotubes. Here the situation is more complicated since electron transport through the tube has to be enabled prior to characterizing the contact quality. This is typically done in a *transistor-like* three-terminal configuration where a gate electrode is used to accumulate charge on the semiconducting tube thus allowing current transport through the same. When a metal/nanotube/metal system is investigated in this way, one would in general expect a Schottky barrier at the metal/nanotube interface to have a significant impact on the current flow. For a *regular type* 3-D metal / 3-D semiconductor interface (without a significant number of interface states) one could expect the barrier height to vary with the work function difference between the two materials. Following this argument, a number of groups have contacted semiconducting nanotubes with high work function metals as Ni or Au assuming that barrier free hole injection into the valence band of the nanotube would become possible [18], [19]. In fact, their results seem to support their assumption. Output as well as transfer characteristics strongly resemble those of conventional, barrier-free MOSFETs (see Sections below). On the other hand, recent studies on the impact of annealing versus doping of tubes [20], experiments on ambipolar nanotube devices [21], and detailed studies of transistor characteristics as a function of temperature and dielectric film thickness [22] support the existence of Schottky barriers and their importance for the current transport in carbon nanotube transistors. The controversy about the impact of contact barriers in carbon nanotube transistors is not yet settled. Further work will finally reveal the true nature of carbon nanotube/metal contacts.

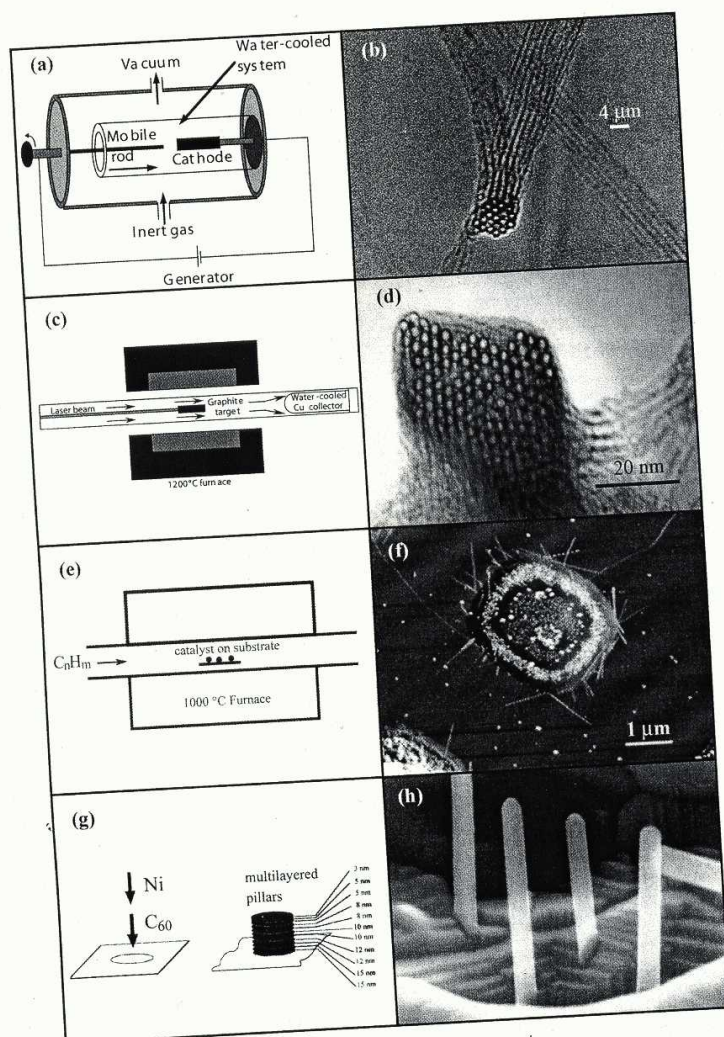
### 3 Synthesis of Carbon Nanotubes

Single-wall carbon nanotubes (SWNTs) can be produced by several methods. Mass production and processing are still serious obstacles toward many proposed applications in industry, and the fabrication of ordered nanotube arrays with full control over their structural and electronic properties remains a major challenge toward applications in nanoelectronics. Consequently, both the synthesis and the assembly of carbon nanotubes continue to be hot research topics and new procedures are continuously being reported. Here, we focus on a few of the most common or promising methods of synthesis, processing and assembly of SWNTs, with a special emphasis on those that are more relevant for nanoelectronics.

#### 3.1 Synthetic Methods

##### Electric arc discharge

The first carbon nanotubes, discovered by Iijima in 1991 [1] were multi-wall carbon nanotubes (MWNTs), as described in the beginning of the chapter. These nanotubes were produced by an arc-discharge method similar to the one that was earlier used to synthesize the famous football-shaped  $C_{60}$  molecule [23]. The method consists of applying a voltage between two graphite electrodes held close together in a chamber filled with an inert gas. The electrical discharge that takes place between the electrodes heats up the region to thousands of degrees, leading to the evaporation of carbon. The carbon vapor crystallizes on the end of the negative electrode, forming MWNTs with diameters ranging between 4 and 30 nm. The introduction of small amounts of transition metals such as Fe, Co, and Ni lead to the formation of single-wall carbon nanotubes (SWNT) [24], [25]. As an example for an efficient SWNT production method, the arc discharge apparatus of Journet et al. [26] is schematically depicted in Figure 15a. Highest yields



**Figure 15:** Synthetic methods for the production of single-wall carbon nanotubes:

(a) – (b) Electric arc discharge, and TEM image of the product;  
 (c) – (d) Laser vaporization, and TEM of the product;  
 (e) – (f) Chemical vapor deposition; and SEM image of SWNTs grown from lithographic catalyst islands on a Si wafer.  
 (g) – (h) Fullerene recrystallization, and TEM of the product (the rods have a diameter of ~40 nm).

(70 – 90 %) of SWNTs were obtained by filling the positive graphite electrode with 1 % Y and 4.2 % Ni, and gradually screwing it toward the negative electrode during the reaction, in order to keep a constant voltage drop of 30 V with a current of 100 A. The SWNTs in Figure 15b show an average diameter of 1.4 nm, and form crystalline ropes very similar to the ones obtained by the laser vaporization method.

### Laser vaporization

A high-yield (70 %), large-scale production of SWNTs is also achieved by the laser-vaporization method which has been first reported in 1996 by the group of Smalley [27]. In this method, represented in Figure 15c, a target of graphite containing small amounts of Co and Ni powder is placed in the middle of a tube furnace at 1200 °C under a flow of argon, and hit by a series of laser pulses. With every laser pulse, a plume of carbon and metal vapors emanates from the surface of the target, and nanotubes start to grow in the gas phase. The nanotubes continue to grow while flying downstream along the tube, until they exit the furnace and are collected on a cold finger as a spongy black deposit. Each fiber of this material consists of a rope of 100 to 500 parallel SWNTs, close-packed as a two-dimensional triangular lattice, as shown in Figure 15d. This pulsed-laser ablation synthesis afforded SWNTs in large amounts, which made many physical and chemical studies possible for the first time, and it is still the production method preferred by several companies that commercialize carbon nanotubes.

### Chemical vapor deposition

Both the electric arc discharge and laser vaporization methods produce ropes of SWNTs. The first production of individual SWNTs was reported in 1998 by the group of Hongjie Dai [28] and was based on a CVD technique (Figure 15e). SWNTs were grown *in situ* on silicon wafers having lithographically patterned catalytic islands of alumina ( $\text{Al}_2\text{O}_3$ ) powders containing Fe and Mo catalytic nanoparticles. These substrates were placed in a tube furnace at 1000 °C under a flow of methane. The hydrocarbon worked as a carbon precursor, which decomposed on the catalyst, and the carbon crystallized in the form of individual SWNTs emerging from the catalyst islands. This simple CVD procedure opened up the possibility of producing prototype *nanotube chips* by growing individual SWNTs *in situ* on specific locations on a flat substrate (example: Figure 15f, see also Figure 18) and, hence, may prove very useful for *in situ* production of nanotube assemblies and nanocircuitry. It was also found that other gases could be used as carbon precursors, including carbon monoxide (CO), ethylene ( $\text{C}_2\text{H}_4$ ) and benzene ( $\text{C}_6\text{H}_6$ ) [29].

### Fullerene recrystallization

SWNTs produced by the above-mentioned methods consist of random mixtures of nanotubes with different diameters and chiralities, that can be either metallic or semiconducting. This structural and electronic variety is a serious obstacle toward the application of SWNTs in nanoelectronics. A new synthesis method, reported in 2001 [30] has been the production of homogeneous single crystals of SWNTs by alternated layers of Ni and  $\text{C}_{60}$  evaporated on Mo or Si substrates through a shadow mask, forming an array of  $\text{C}_{60}/\text{Ni}$  multilayer pillar. However, detailed studies have shown that this initial idea proved to be not correct and different phases to be formed instead of SWNTs [31].

## 3.2 Growth Mechanisms

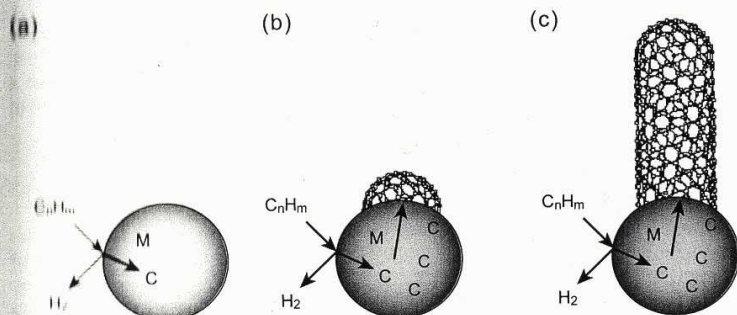
The mechanism of SWNT growth is still a debated issue. Since SWNTs were first observed, several growth mechanisms have been proposed, although none of them has yet received definitive experimental or theoretical support.

### Catalytic vs. vapor-liquid-solid model

Initially, the fact that transition or rare metals, or mixtures of them, were always required for the formation of SWNTs, led to the proposition of catalytic mechanisms involving the coordination of metal atoms to the dangling bond of the growing nanotubes. Such was, for example, the *scooter mechanism* [32], where transition metal atoms bridging between two carbon atoms would go *scooting* around the edge of the nanotube, as it is growing. A rather different mechanism was based on the vapor-liquid-solid (VLS) macroscopic model, which was known from the 1960s to explain the growth of Si whiskers. In the VLS model, growth occurs by precipitation from a super-saturated catalytic liquid droplet located at the top of the filament. The atomic catalyst models were earlier supported because it was understood that if the VLS mechanism were correct, a catalyst particle should be left at the end of each nanotube, and this had not been observed. More recently, however, both the controlled growth of SWNTs from individual nanoparticles [33] by the CVD method, and meticulous observation of SWNT ropes under the TEM [34], allowed the unequivocal observation of metal clusters at the ends of SWNTs. Since then, a very plausible mechanism is actually a combination of the catalytic and the VLS models, referred to as the *root-growth mechanism*.

### Root-growth mechanism

The root-growth mechanism for the growth of an individual SWNT from a metal nanoparticle on a substrate by the CVD method is schematically represented in Figure 16. 16. First the hydrocarbon decomposes on the metal nanoparticle into hydrogen and carbon, which dissolves in the metal (Figure 16a). When the carbon becomes super-saturated in the nanoparticle, it starts to precipitate in the form of a graphitic sheet. Since the edges of the graphitic sheet are unstable, the emergence of *pentagon defects*, leading to the for-



**Figure 16:** Root-growth mechanism for the formation of a single-wall carbon nanotube from a metal nanoparticle, by chemical vapor deposition:

(a) decomposition of the hydrocarbon on the nanoparticle and solubilization of the carbon therein.

(b) nucleation by formation of a fullerene cap.

(c) elongation of the SWCNT by incorporation of further carbon into the metal-carbon bonds at the growing end.

formation of a curved fullerene cap (Figure 16b), becomes energetically favored, as it allows the dangling bonds of this cap to be stabilized by coordination with the metal. As in the catalytic models, the interaction between the partially filled 3d orbitals of the transition metal and the empty  $\pi^*$  orbitals of the carbon, may play a crucial role in stabilizing the dangling bonds of the fullerene cap. After the cap is formed, two things can happen. In one case, as shown in Figure 16a, more carbon atoms can insert into the metal-carbon bonds, leading to the elongation of the fullerene, and the growth of a SWCNT. Otherwise (not shown), the fullerene cap can keep growing around the nanoparticle, eventually engulfing it, and preventing any further growth. The competition between these two pathways should determine the yield of SWCNT growth. An analogous mechanism has been proposed for the growth of SWCNT ropes from larger metal nanoparticles from carbon vapors, produced either by arc discharge or laser vaporization.

### 3.3 Processing and Functionalization

SWCNTs obtained by both arc discharge and laser vaporization, are usually decorated with a significant fraction (10–30%) of nanoscale impurities, including amorphous carbon, bucky onions, spheroidal fullerenes and residues of the metal catalyst. A convenient way of *purifying* these as-made SWCNTs consists of first refluxing the material in nitric acid ( $HNO_3$ ), and then suspending the nanotubes in a basic aqueous solution of a non-ionic surfactant followed by cross-flow filtration [35]. The resulting suspension is passed through a Teflon filter, and a black mat or *bucky paper* is peeled off the filter. This bucky paper consists of a dense tangle of clean SWCNT ropes. These ropes usually have a length of several microns.

SWCNTs are extremely insoluble in any solvent. In addition, the strong Van der Waals forces keep nanotubes aggregated in ropes and tangles. SWCNT ropes can be suspended in aqueous solutions with appropriate surfactants, as mentioned above, but the ropes will usually not break apart into well-separated SWCNTs. *Suspensions* of SWCNTs in organic solvents were first obtained with thionyl chloride and octadecylamine [36]. Natural polymers extracted from the acacia tree have been used successfully to stabilize individual SWCNTs in aqueous solutions [39].

Nanotubes are quite inert to covalent functionalization. *Covalent functionalization* of the nanotube sidewalls was only achieved by reaction with very reactive species, such as radicals, carbenes and nitrenes [37]. Otherwise, the non-covalent sidewall functionalization was obtained by adsorption of polycyclic aromatic hydrocarbon groups, which served for anchoring proteins to the nanotubes [38]. At the open end, nanotubes are somewhat more reactive. The terminal C atoms can be oxidized to carboxylic groups which can be used for typical chemical synthesis strategies.

### 3.4 Assembly of Nanotube Arrays and Nanocircuitry

For nanotubes to be used in nanoelectronics, it is the ability to assemble and integrate them in nanocircuitry, rather than mass production, what constitutes the most critical issue. Another important aspect is the control of diameter and chirality, or at least a selection between metallic and semiconducting nanotubes, which will play different roles in nanocircuitry.

#### Controlled deposition from solution

SWNT arrays lying on a surface have been produced by selective deposition on functionalized nanolithographic templates [40]. In spite of initial success, the extension of this *wet* approach proved to be rather difficult due to the tendency of SWNTs to aggregate due to van der Waals interactions. It is just hard to find anything that nanotubes would like to stick to, better than to each other. Nonetheless, if SWNT ropes are good enough for a particular use, microfluidics combined with electric fields has produced nice crossbar arrays of SWNT ropes [41] as shown in Figure 17a. With the recent discovery of new ways of suspending individual SWNTs, as mentioned above, the assembly of nanotube arrays by *wet methods* may now become more feasible.

#### Controlled growth of suspended networks

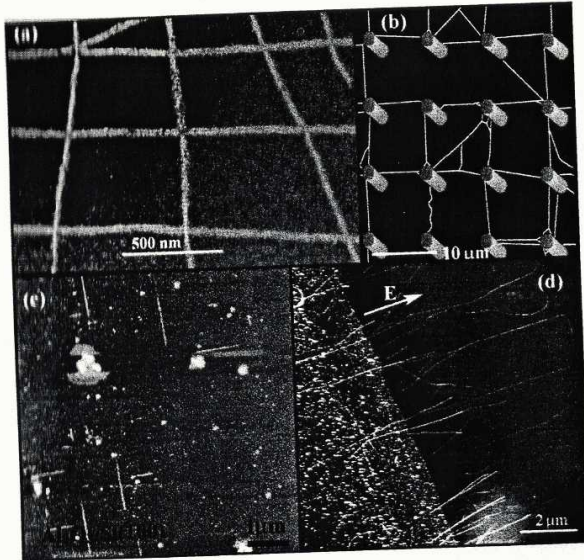
After the discovery that individual SWNTs could be grown *in situ* on silicon wafers by the CVD method, **controlled growth** became an attractive alternative to **controlled deposition**. The *in situ* approach has the advantage that it avoids nanotube aggregation. Dai et al. found that when SWNTs were grown from catalytic islands deposited on the top of microfabricated pillars, nanotubes stretched from one pillar to the next one, and so forth, forming amazing suspended networks, as shown in Figure 17b, [42]. Presumably, when a nanotube is growing from the top of a pillar, it "waves around" in every direction, but when it touches the top of another pillar, it gets pinned to it. Then, the same nanotube can keep growing and jumping from pillar to pillar for more than 100  $\mu\text{m}$ . This approach can be used to build different nanotube architectures. The directionality of suspended SWNTs could also be enhanced by applying an electric field [43].

#### Lattice-directed growth

An interesting approach to the directional growth of supported SWNTs, was developed by Liu et al. [44], who found that when SWNTs were grown by CVD on etched Si wafers, the nanotubes preferred to grow parallel to the lattice directions of the crystalline surface. Thus, when SWNTs were grown on Si(100), the nanotubes were lying with angles of  $90^\circ$  and  $180^\circ$  between each other as shown in Figure 17c. On the other hand, when SWNTs were grown on Si(111), the nanotubes were lying with angles of  $60^\circ$  and  $120^\circ$  between each other. This directionality could be explained by the specific interactions of the SWNTs with the aligned rows of Si atoms of the wafer. This procedure may, in principle, lead to supported nanotube crossbars. However, it is not clear yet if surface growth allows nanotubes to cross each other as they are both interacting with the surface.

#### Vectorial Growth

An approach for the production of supported nanotube arrays, reported by Joselevich et al. [45] is the concept of vectorial growth, where the growth of SWNTs lying on a surface is geometrically defined as a vector, having a particular position, direction and length. Ideally, one would also like to have control over the diameter and the chirality of the nanotubes, which determine whether they are metallic or semiconducting. SWNTs were produced *in situ* by CVD on Si wafers under the action of a local electric field parallel to the surface. The origin of the growth vector is defined by the position of patterned catalyst nanoparticles, while the direction of vectorial growth is defined by the electric field that is created by a pair of lithographic microelectrodes. The length is determined by the reaction time, and the diameter can be controlled by the catalyst nanoparticle size. When the nanotubes are longer than a critical size of the order of a micron, most nanotubes are well aligned with the electric field (Figure 17d). However, when the nanotubes are shorter than the critical length, only the metallic nanotubes are well aligned along the field, while the semiconducting ones are found in completely random orientations. This finding is consistent with theoretical calculations which showed



**Figure 17:** Methods for the assembly of carbon nanotube architectures:  
 (a) Controlled deposition from a polymer-stabilized organic solution in a microfluidic system with applied electric fields.  
 (b) Controlled growth of suspended structures from pillars.  
 (c) Lattice-oriented growth on Si(100).  
 (d) Vectorial growth from patterned catalyst nanoparticles under an electric field.

that when nanotubes are shorter than the critical length, only the metallic ones attain an induced dipole that is large enough to overcome the thermal fluctuations. Hence, sequential steps of vectorial growth could be used to produce complex and robust nanocircuits. Moreover, this method may provide a means of selective synthesis or separation of metallic and semiconducting nanotubes, which is very important toward the application of carbon nanotubes in nanoelectronics.

#### 4 Carbon Nanotube Interconnects

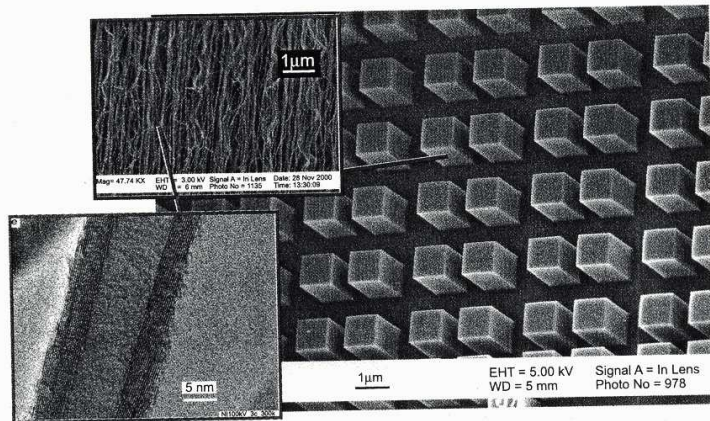
The lateral scaling of dimensions in silicon technology affects the transistors as well as their interconnects. In modern technology generations, chip wiring is produced using the damascene technique, where grooves are etched into a dielectric layer and subsequently filled with copper. Chemical mechanical polishing is used to remove the excess copper above the grooves. The result resembles inlay work or the patterned structure on a damascene sword which lends its name to the technique (see Chap. 29).

Scaling the width of the lines increases the resistance, not only because of the reduced cross section, but also due to increased scattering from the surface and the grain boundaries [46]. This problem can not be addressed by material innovation because the only metal with better bulk conductivity than copper is silver with only a 10 % improvement. If, however, wires could be made without intrinsic defects and with perfect surfaces, additional scattering might be avoided.

Carbon nanotubes may fulfill these requirements to a large extent. They offer unparalleled translational symmetry in one dimension with an intrinsically perfect surface. For metallic nanotubes the electron density is high and the conduction is easy along the tube axis due to the  $\pi$ -electron system. Moreover, it has been shown [50] that electron transport along the tubes is ballistic within the electron-phonon scattering length, which is of the order of micrometers at room temperature [17], [48] (Sec. 2.4). The absence of scattering also allows for much higher current densities than in metals.

Carbon nanotubes can be grown in different ways as described in Sec. 3. Most suitable for microelectronic applications is the catalyst mediated CVD growth [49]. This method can be used to grow CNTs at predefined locations if the catalyst is patterned by lithographic methods (Figure 18).

**Figure 18:** Nanotube blocks created by catalyst mediated growth. The tubes are generated from iron catalyst pads ( $100 \times 100 \mu\text{m}$ ) patterned by the lift-off technique. The first inset shows that each block consists of numerous nanotubes with a length exceeding  $100 \mu\text{m}$ . The second inset shows a TEM-image of a single nanotube revealing that the tubes are multi-wall with about 16 shells and a diameter of approximately  $20 \text{ nm}$ .

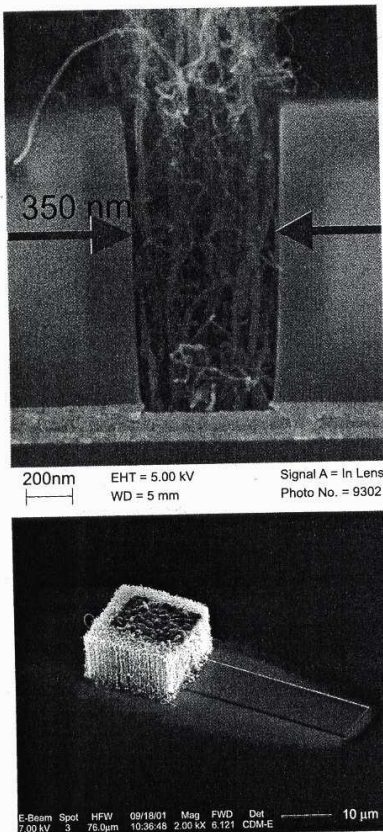


#### 4.1 Nanotubes in Vias

If nanotubes can be grown on a metal substrate in a similar way, they could also be produced in vias, which are the interconnects between two metallic layers. Vias are always prone to material deterioration such as void formation and subsequent breakdown because of the high current densities in small holes and current crowding effects at the edges. Nanotubes, that serve as interconnects in vias, would be much less susceptible to damage due to high current densities and permit vias to be made with smaller diameter.

Figure 19 (top) shows a SEM cross section through a via. The bottom contact is tantalum covered with the catalyst. It should be noted that the morphology of the catalyst plays a dominant role in nanotube growth and the deposition process must not change the catalyst's structure. It can be seen that the nanotube growth is selective and homogeneous in the via. Figure 19 (bottom) a tungsten top contact has been formed by a focussed ion beam deposition.

The electrical characterisation of the nanotube via is shown in Figure 20. The current-voltage characteristic is ohmic indicating good contact between the nanotubes and the metal layers. Obviously the majority of the nanotubes contacted are metallic or semiconducting with high conductivity. An estimation of the number of tubes involved yields an average resistance per tube of  $10 \text{ k}\Omega$  which is close to the optimum resistance of one shell and one spin degenerate conduction level [50]. Most probably more than one shell per tube contributes to the conductance, giving rise to additional conductive channels.



**Figure 19:** Homogenous selective growth of nanotubes in a narrow via. The bottom layer metal is tantalum covered by  $\text{SiO}_2$  dielectric (top). The top contact is formed from a FIB-deposited tungsten layer (bottom).

#### 4.2 Maximum Current Density and Reliability

Ballistic transport in a carbon nanotube implies that no scattering occurs within a characteristic scattering length. The power dissipation will be restricted to the contact region if the wire length does not exceed this scattering length. The nanotubes themselves should exhibit a much higher maximum current density than a polycrystalline metal. This has been confirmed in many publications where current densities up to  $10^{10} \text{ A/cm}^2$  have been reported [55].

To date the reliability of multi-wall nanotubes has not been investigated systematically. However, first attempts, reported in ref. [56], have been made to monitor the maximum current as a function of time at elevated temperatures in air. Both tubes investigated carried current densities of  $5 \times 10^9 \text{ A/cm}^2$  and  $2 \times 10^{10} \text{ A/cm}^2$  for more than 300 h. For comparison, copper interconnects fail at current densities of  $\sim 10^7 \text{ A/cm}^2$ . This result shows that carbon nanotubes have intrinsically much higher strength against deterioration effects like electromigration than metals.

#### 4.3 Signal Propagation in Nanotubes

Signal propagation in conventional ohmic wires is determined by the propagation velocity of an electromagnetic wave in a dielectric and by the signal rise-time influenced by the resistance, the capacitance and the inductance of the wire. The exact treatment of signal propagation in nanotubes is a sophisticated task. However, for a first estimation of

the difference, between a classical ohmic wire and a nanotube we consider the nanotube as a wire with a length-independent resistance and a capacity that is modified by the electrochemical capacity to account for the intrusion of the electric field into the nanotube [57]. If we approximate the capacity for both ohmic and nanotube wires in the coaxial cylinder configuration, and neglect inductance and interaction with drive and load transistors, we can deduce the interconnect delay as function of the wire length [47]. Figure 21 shows the delay of a set of ohmic wires (black lines) with different cross sections  $A$ . The wires with cross sections smaller than  $(100 \text{ nm})^2$  are corrected for additional surface scattering effects [46]. The nanotube case is represented by the two blue lines for quantum wires with two ( $M=2$ ) and ten ( $M=10$ ) occupied energy levels. The  $M=10$  case also represents a multi-wall nanotube with, e.g., five shells and two occupied energy levels in each shell. It can be easily seen that a multi-wall nanotube might show less delay than an ohmic wire of  $(10 \text{ nm})^2$  cross section for wire lengths  $> 300 \text{ nm}$ . Thus, beneficial applications in nanoelectronics would be metallic multi-wall nanotubes with large diameters (large number of occupied levels).

## 5 Carbon Nanotubes Field Effect Transistors (CNTFETs)

### 5.1 Comparison to MOSFETs

The success of modern silicon technology is owed, to a large extent, to MOSFETs and the CMOS concept in which circuits draw current only during the switching action and are thus the indispensable ingredients for low power complex circuits like processors and controllers. The inversion channel of MOSFETs can be considered as a 2-D conduction system. Electron motion in the inversion channel is not *a priori* restricted in planes but due to high gate fields the motion perpendicular to the gate plane is quantized giving rise to subband formation. The conductive channel can be considered as a 2-D electron gas. At room temperature many subband levels contribute to the current transport enabling a high driving capability and switching speed.

Semiconducting carbon nanotubes can be operated in a gate electrode configuration in a similar way to silicon MOSFETs. The electronic properties of CNTs have been described in Sec. 2. The excess electrons are delocalized and form a highly conductive 1-D electron system. Unlike in silicon MOSFETs the electron system of a nanotube is 1-D. Placing a field electrode next to the nanotube one can influence its conductivity by the accumulation or depletion of electrons provided that the electron density is not too high (the tube is semiconducting). This configuration is called CNTFET, in analogy to the silicon field effect transistor. As the electrical characteristics of carbon nanotubes strongly depend on their chirality, diameter and doping, the characteristics of CNTFETs can be controlled by choosing the appropriate morphology of the CNT. Single-wall semiconducting tubes are best suited for CNTFETs because their electron system is not bypassed by inner shells.

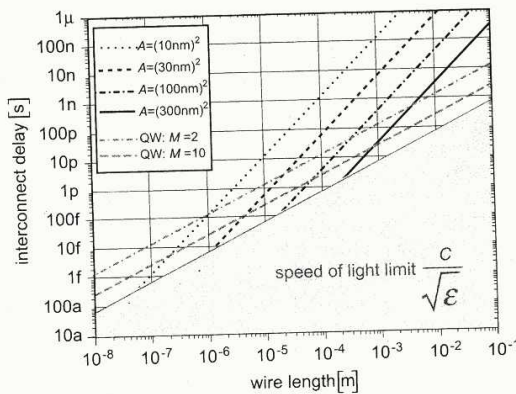


Figure 21: Signal delay in ohmic and ballistic wires as a function of wire length. The black lines represent the delays of ohmic wires with different cross sections  $A$ . Surface scattering has been taken into account. For wire lengths smaller than the intersections of black and red lines, the delay is governed by the speed of light and the relative permittivity of the dielectric. The nanotube wires display a completely different behavior to the ohmic wires, as shown by the blue lines. Due to the length-independent resistance, nanotubes exhibit better delay values for longer wires.  $M$  represents the number of conductive channels, that can be formed either by the number of occupied energy levels or by the number of shells of a multi-wall nanotube.

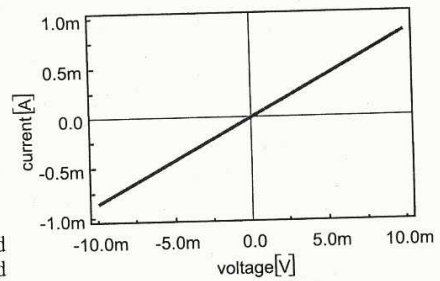
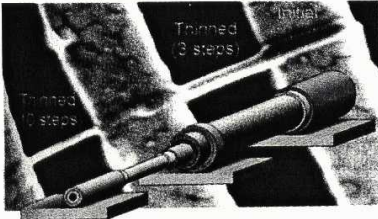
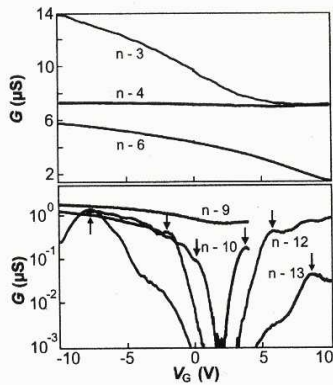


Figure 20: Current-voltage characteristic of a via filled with nanotubes. Ohmic behaviour is observed.





**Figure 22:** Controlled burn-off of the individual shells of a multi-wall nanotube between three adjacent contacts. In the first section three shells have been removed whereas ten shells have been stripped in the second section. The SEM picture and inset with schematic drawing are taken from [62].



**Figure 23:** Conductivity of individual shells of a multi-wall nanotube (taken from [62]). The shells are removed by controlled current induced burn-off. The outermost shells show high conductivity with shell n-4 being metallic (top). As the diameter of the shells decreases, the conductivity at constant bias voltage  $V_G$  decreases likewise. The innermost shells show a pronounced gate voltage dependence and a widening of the energy gap, in accordance with theoretical expectations (bottom).

## 5.2 Tailoring of Nanotubes

The production of single-wall nanotubes and their deposition is still a matter of arduous work and is by no means compatible with the requirements of a controlled and reproducible parallel production which is characteristic of integrated circuit (IC) technology processes. For IC technology an appropriate number of nanotubes with predefined characteristics must be placed at desired locations in a reproducible way. One step towards this goal is to use custom designed multi-wall nanotubes instead of the single-wall species. Since the diameter as well as the chirality of the shells determines the energy gap and the conduction type of each individual shell, it should be possible to choose the desired characteristics by contacting the appropriate shell. This was realized by a group at IBM who managed to successively burn-off the outer shells of a MWNT located on contacts [62]. The outer shell turned out to be the dominant conductive channel. Figure 22 shows a SEM picture of a multi-wall carbon nanotube placed on top of three contact strips. By applying a controlled current to the tube between two adjacent contacts it is possible to burn-off individual shells within this section by oxidizing them in air, as depicted in the sketch. After manipulating the carbon nanotube in the above described manner it was possible to investigate the electrical conductivity with a back-gate electrode.

Figure 23 shows the conductivity of the tube as a function of the back-gate voltage for 13 different shells that have been successively removed. The three outermost shells were burned-off between the right electrode pair whereas further thinning was done between the left pair of electrodes. The conductivity variation with the gate voltage is quite different for each shell, reflecting the different morphology of each layer. The outermost shell responds to the gate voltage, indicating its semiconducting nature whereas the next shell is metallic with no response. Note that the conductivity decreases as the tube diameter diminishes and that the innermost shells clearly show semiconducting behavior (The conductivity in the bottom diagram is displayed on a logarithmic scale). It can even be deduced that the energy gap widens as the tube diameter decreases, as expected from theory (see Sec. 2).

Figure 24 displays the current-voltage characteristics for high source-drain voltages. It can be seen that for each shell the current saturates and that each saturation value contributes equally in the high current case. For the innermost shells, and at smaller source-drain biases, an exponential behavior can be deduced which originates from tunneling contacts between outer and inner shells in the contact region.

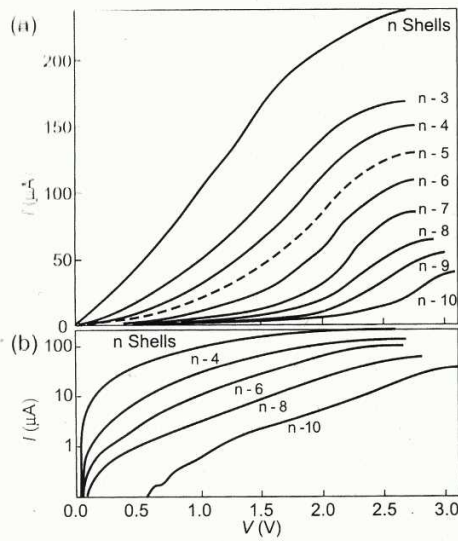
This experiment provides a deep insight into the transport mechanisms in multi-wall nanotubes, at least a qualitative one. Moreover, to solve the problem of arranging the predefined types of nanotubes at the desired locations, it might also be feasible to deposit a multi-wall species and design the required characteristics by the controlled burn-off of individual shells. Thus, certain sections of the same tube can be defined to act as metallic interconnects, whereas others can perform as semiconducting FET devices. It can easily be imagined that circuits with higher complexity might be assembled exploiting controlled breakdown, at least for demonstrators.

It was also shown in [62] that a bundle of single-wall tubes with arbitrarily mixed conduction types can be separated from the metallic species by applying a back gate voltage to drive the semiconducting ones into depletion, while burning-off the metallic ones by an appropriate source-drain voltage.

## 5.3 Back-gate CNTFETs

Having at hand the deposition techniques described in the previous sections for single-wall nanotubes and multi-wall nanotubes as well as the possibility to manipulate individual shells of multi-wall tubes we can now begin to construct carbon nanotube FETs. The simplest arrangement is to place a nanotube on top of a silicon wafer covered with a silicon dioxide dielectric layer. After contacting both ends of the nanotube with an appropriate electrode we can apply a gate voltage at the silicon bulk acting as an overall gate electrode. Tans et al. [58] were the first to investigate a carbon nanotube device which was modulated by a planar gate electrode and operated at room temperature. Slightly later two other groups presented similar results [28],[59]. In all three cases, the CNTs turned out to be p-type conductors.

The arrangement used by Tans et al. [58], which is shown in Figure 25, consists of a single-wall nanotube located on top of two platinum strips which serve as source and drain electrodes. The tube and the contacts are separated by a 300 nm thick  $\text{SiO}_2$  layer grown thermally on top of a silicon wafer that acts as a back-gate electrode. The single

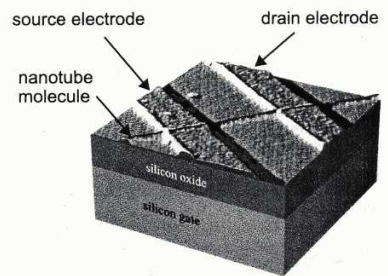


**Figure 24:** Conduction of individual shells of a multi-wall nanotube for the high bias case. The current is driven into saturation and the saturation value of each shell is  $\sim 20$  nA. In the semi-log plot (bottom) exponential current behavior is observed for the innermost shells, most probably resulting from tunneling contacts between the shells in the contact region.

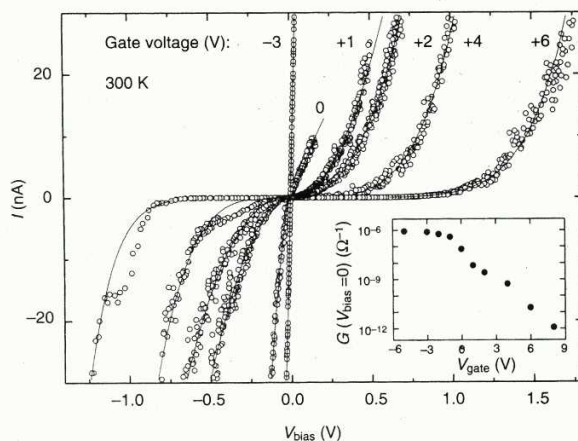
Wall nanotubes were deposited from solution and lie on the contacts by chance. The authors managed to measure about 20 nanotubes, some of them showing metallic behavior with no dependence on the gate electrode voltage and linear current-voltage characteristics. Those showing gate electrode responses were identified as semiconducting and were used for further characterization.

Figure 26 shows the current-voltage characteristics of a single tube for a range of back gate voltages. It can be seen that for positive gate voltages no current flows for small source-drain voltages. By increasing the source-drain voltage a nonlinear current-voltage dependence can be observed for both polarities indicating an energy gap-like behavior with no energy states available for positive gate voltages and small biases. Decreasing the gate voltage to negative values opens the conductive channel even for small source-drain voltages. The insert in Figure 26 reveals that the conductance can be modulated over 6 orders of magnitude for small source-drain voltages, a behavior which is comparable to a silicon MOSFET. The saturation value of the resistance is similar to the resistance of the metallic nanotubes measured in the same experiment ( $\sim 1$  M $\Omega$ ). The major part of the resistance is attributed to the contact resistance as one would expect a value close to the quantum resistance of  $6.5$  k $\Omega$  for a spin degenerate system with two occupied energy levels [50].

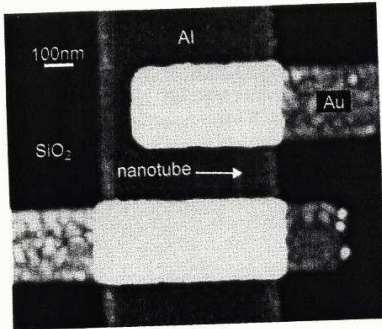
The presentation of the CNTFET by Dekker's group in 1998 set a landmark in the development of nanoelectronic devices since, for the first time, the function of a device with nanometer dimensions was demonstrated at room-temperature and which exhibited similar or even better characteristics than those expected for silicon-transistors with equivalent dimensions.



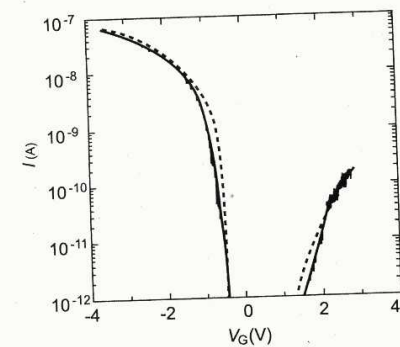
**Figure 25:** A carbon nanotube field effect transistor (CNTFET). The nanotube (red) is located on top of two platinum contacts (yellow). The back-gate-stack (blue) is formed by a silicon dioxide dielectric on top of a silicon wafer (colored AFM-image taken from [58]).



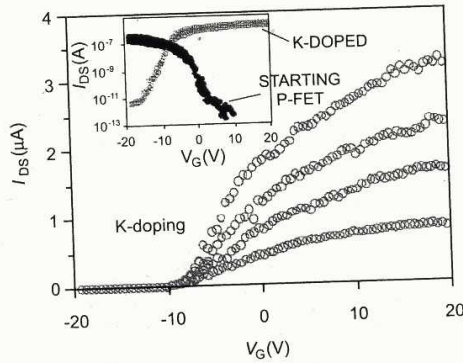
**Figure 26:** The current-voltage characteristics of a semiconducting single-wall carbon nanotube for different gate voltages (see Figure 25). For large positive gate voltages the conductance of the tube is very small for source-drain biases less than approximately 1 V. Changing the gate voltage to negative values increases the conductivity steadily until saturation is reached at approximately  $-3$  V (see insert). The maximum conductivity is comparable to the values found for metallic tubes measured in the same experiment (taken from [58]).



**Figure 28:** Isolated back-gate CNTFET. The gate is realized by an Al-strip on top of SiO<sub>2</sub>. The gate oxide is the naturally grown thin Al<sub>2</sub>O<sub>3</sub> layer on top of the Al-strip. Source and drain contacts are made by Au deposition ([65]).



**Figure 29:** Source-drain current of a single-wall nanotube on Al<sub>2</sub>O<sub>3</sub> gate dielectric for a source-drain voltage of 5 mV. p- and n-channels can be opened by altering the gate voltage (after [65]).



**Figure 27:** Inversion of the conductivity type of a semiconducting carbon nanotube. As displayed by the insert the starting device was a p-type CNT-FET. After exposure to potassium vapor, the conductivity type was reversed with current flowing for positive gate voltages (after [64]).

### 5.4 Complementary Carbon Nanotube Devices

As mentioned, the CNTFETs presented up to now were p-type only! As in silicon technology, however, it is highly desirable to have both p- and n-type CNTFETs available. Only complementary arrangements, for which one transistor always is in the off-state, show sufficiently low power consumption for large scale integration circuitry.

For carbon nanotubes the fabrication of p-n junctions within one nanotube has been achieved by covering one part with a resist and exposing the uncovered part to potassium vapor [51]. The first appearance of n-type behavior of nanotube ropes under positive back-gate bias was reported by Bockrath et al [52]. They also used potassium vapor in a doping vessel to diffuse donor atoms into the former p-type nanotubes. Following the concept of doping, Collins et al. [53] and Bradley et al. [54] interpreted the earlier results on p-type devices as unintentional oxygen doping of carbon nanotubes. However, it was not perfectly clear at that point, why only either electron or hole transport was observable and no ambipolar characteristics could be obtained despite the small band gap in case of nanotubes of only 0.6 eV. Martel et al were the first to succeed in producing CNTFETs with ambipolar conduction character depending on the polarity of the gate voltage. Their devices had Ti/TiC contacts providing sufficiently low barrier heights for both hole and electron transport. In addition, a thin SiO<sub>2</sub> passivation layer was used for stable operation in air [21].

Derycke et al. [64] used potassium doping to reverse the conduction type of a CNT-FET. Figure 27 (insert) shows the conversion of an originally p-type nanotube FET to n-type by K-doping and the resulting  $I_{DS}$  versus  $V_G$  characteristics. Potassium acts as an electron donor shifting the Fermi-level to the conduction band. As a result, the concentration of electrons in the conduction band increases for positive gate voltages. The IBM group was also able to prove that pure n-type nanotube behavior can be obtained by annealing devices in vacuum. The results were discussed as a consequence of the presence of Schottky barriers and their sensitivity to ambient gases such as oxygen. Nowadays understanding is that a combination of bulk doping and contact effects is likely to be responsible for the transport properties observed in nanotube devices.

### 5.5 Isolated Back-Gate Devices

The CNT-devices discussed so far were controlled by a common back-gate stack which consists of a thermal oxide layer on top of a doped silicon wafer. Thus, the gate electrode extends over the whole silicon wafer and covers also the large contact pad areas. Due to the risk of defects resulting in high leakage currents or circuit shorts the gate oxide thickness must be kept in the 100 nm range. An effective gate control can therefore only be achieved with high gate voltages and the gain of most devices is smaller than unity. However, the Delft University group succeeded in constructing an isolated back-gate device by exploiting thin, naturally grown Al<sub>2</sub>O<sub>3</sub> on top of a patterned aluminum electrode as gate oxide with a thickness of a few nanometers [65]. The basic device is displayed in Figure 28. Source and drain electrodes are patterned by electron-beam lithography and subsequent metal deposition and lift-off on top of a 1 nm diameter single-wall nanotube pre-selected and positioned by AFM.

In Figure 29 the drain current for a fixed source-drain voltage is shown as a function of the gate voltage. Obviously the Fermi-level is shifted by the gate voltage from the valence band (accumulation) over the gap (depletion) into the conduction band (inversion). The conductance type can be varied electrostatically by the gate voltage from p-type to n-type. The minimum resistance can be deduced at high negative gate voltages to be 80 k $\Omega$ , indicating good contacts.

In Figure 30 the  $I/V_{sd}$  characteristics of a CNTFET are shown for different gate voltages. Saturation behavior similar to a silicon-MOSFET can be clearly seen. The gain of this device exceeds 10, making it suitable for driving other devices. The transconductance is approx. 0.3  $\mu\text{S}$  and the on/off ratio covers more than 5 orders of magnitude. The maximum current is of the order of 100 nA, equivalent to a current density of approx.  $10^7 \text{ A/cm}^2$  with an on-resistance of 26 M $\Omega$ .

### 5.6 Isolated Top Gate Devices

A further step towards compatibility with microelectronics was achieved by Wind et al, who presented an optimized CNTFET with Ti/TiC source-drain contacts and a thin (15–20 nm) gate-oxide which was deposited on top of the nanotube [66]. Due to the small thickness of the gate oxide and the top gate arrangement excellent gate control is achieved. Figure 31 shows the schematic cross section of the device and the drain current versus source-drain voltage characteristics. Note that the device can be operated with a gate voltage swing of only 1 V. N-type devices can be fabricated by annealing a p-type tube in inert atmosphere prior to gate oxide deposition. A thin passivation layer capping the device enabled stable operation in air. A record value of 3.25  $\mu\text{S}$  was measured for the transconductance.

### 5.7 Comparison of Si-MOSFETs with up-scaled CNT-MOSFETs

Since their first introduction in 1998 the evolution of CNTFETs has yielded a steady improvement of the electrical characteristics, as has been described in the previous sections. A comparison with state of the art Si-MOSFETs has first been attempted by Martel et al [68]. Their data, as deduced from a back-gate CNTFET with Ti/TiC source-drain contacts, already shows competitiveness to state-of-the-art Si-MOSFETs. The top-gate transistor presented by Wind et al. [66] with carefully designed contacts and gate-oxide, shows unprecedented values for transconductance and maximum current drive (Table 1).

	p-type CNFET	Ref. 59	Ref. 60
Gate length (nm)	260	15	50
Gate oxide thickness (nm)	15	1.4	1.5
$V_t$ (V)	-0.5	$\sim -0.1$	$\sim -0.2$
$I_{ON}$ ( $\mu\text{A}/\mu\text{m}$ ) ( $V_{ds} = V_{gs} - V_t \approx -1 \text{ V}$ )	2100	265	650
$I_{OFF}$ (nA/ $\mu\text{m}$ )	150	< 500	9
Subthreshold slope (mV/dec)	130	$\sim 100$	70
Transconductance ( $\mu\text{S}/\mu\text{m}$ )	2321	975	650

Table 1: Comparison of most important transistor data for a p-type CNTFET and two advanced Si-MOSFETs (reproduced from [66]).

The data for the CNTFET were deduced from a single nanotube and were virtually upgraded by parallel operation of an appropriate number of tubes to form a two-dimensional arrangement with dimensions comparable to two most advanced MOSFET devices. It has to be kept in mind that a grid of parallel nanotubes has not been realized up to now and that the gate field would be weakened by screening of densely packed tubes. There is also a difference in channel length between both devices. Assuming ballistic transport CNTFETs should be scalable in length. However, it is still unclear whether the location of the gate relative to the contacts has any influence on the transconductance.

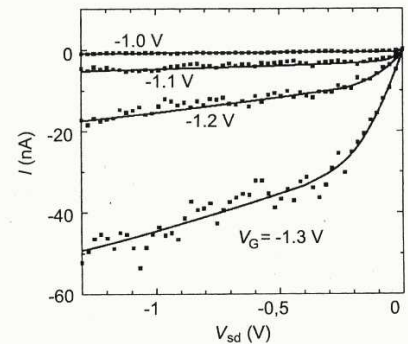


Figure 30: Output characteristics of a p-CNTFET. The drain current shows a saturation-like behavior at large source-drain voltages. The gain is above 10 (after [65]).

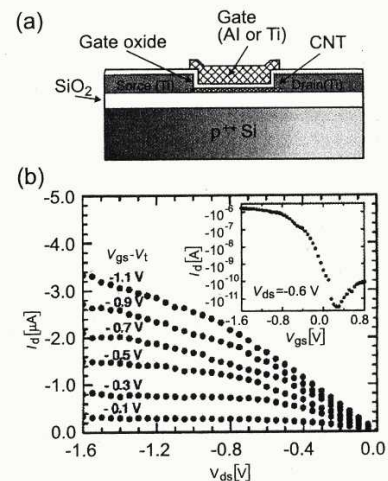
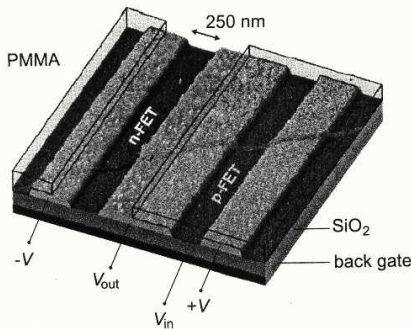


Figure 31: (a) Schematic cross section of a top gate CNTFET. (b) Output characteristics of a p-type device with Ti gate and a gate oxide thickness of 15 nm. Gate voltage ranges from -0.1 V to -1.1 V above the threshold voltage of -0.5 V. The insert shows the gate controlled drain current at a fixed source-drain voltage of -0.6 V [66].



**Figure 32:** Intramolecular complementary CNTFET gate made by an n-type and p-type CNTFET in series, operated by a common back-gate. Complementary transistors are produced from one single nanotube by doping the section which is not covered by the PMMA resist with potassium (after [64]).

It can be seen from Table 1 that, even for transconductance to be half of the values deduced, the CNTFET still outperforms the MOSFETs. Further improvement can also be expected by reduction of the gate-oxide thickness and lowering of the contact resistances at source and drain.

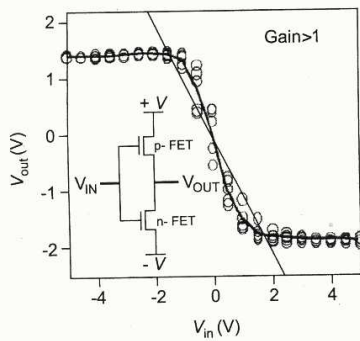
Let us now consider the theoretical limits of a CNTFET. Performing a best case approximation and taking into account that the conductance is independent of the length (ballistic transport), the value for a spin-degenerate one level system is  $153 \mu\text{S}$  per tube (!). Assuming equal lines and spaces and a tube diameter of 1.4 nm the maximum conductance would be more than  $50000 \mu\text{S}/\mu\text{m}$ . This is unrealistically high because contact resistances and gate coupling were not considered. However, improvement of the contact resistance alone will further enhance the nanotube transconductance considerably.

Guo et al. have performed a thorough theoretical treatment of a CNTFET [67]. They showed that a coaxial gate would enhance the transconductance by a factor of 7 as compared to the plane gate electrode used for all devices up to now. They have also found that the maximum transconductance of their n-type device is  $63 \mu\text{S}$  a value considerably higher than the best value reported so far for a p-type device ( $3.25 \mu\text{S}$  [66]).

This comparison shows, that there is lot of room for improvement of current nanotube device technology, which is by no means mature.

### 5.8 Carbon Nanotube Circuits

With the availability of devices with sufficient gain, on-off ratio and driving current separately addressable by a gate voltage, one can realize simple circuits – the first step for integration of CNTFETs. Derycke et al. succeeded in selectively doping part of one single carbon nanotube placed on top of three contacts in a back-gate arrangement by covering a section of the tube with PMMA and exposing the other to potassium vapor or annealing it in vacuum [64]. Figure 32 shows this *intramolecular* gate. The entire nanotube represents a n-type and a p-type FET in series, controlled by a common gate. By applying a gate voltage, either one of the two transistors is in the off-state with no current flowing in both logic high and low states. In Figure 33 the proper operation of the *CMOS-type* gate shown in Figure 32 is demonstrated. It can be seen that the output voltage changes within a narrow input voltage interval centered at 0 V. The straight line marks a voltage gain of 1. The blue line is an average of five consecutive measurements indicating that this device shows a gain higher than unity. This is a prerequisite for driving other gates.



**Figure 33:** Input-output characteristic of a complementary CNTFET gate. The output voltage switches from logical 1 to 0 as the input voltage changes from negative to positive values. Red circles represent the data of five measurements on the same device. The blue line is the average of this measurements indicating a voltage gain  $> 1$  (straight line).

Using the CNTFETs presented in the previous section and combining them with external resistors the Delft University group [65] realized an inverter, as shown in Figure 34 (left). When the gate voltage is switched from 0 V (logical 0) to  $-1.5 \text{ V}$  the output voltage changes from  $-1.5 \text{ V}$  to 0 V. In a similar way, by connecting two CNTFETs in parallel to a common resistor, they realized a NOR gate with the typical input-output scheme as displayed in Figure 34 (right). Due to the high resistances and capacitances involved, switching is slow compared to the typical values of today's microelectronics. However, it should be kept in mind that the switching element itself has lateral dimensions of only 1 nm and the on-resistance has to be compared with the lowest resistance that a quantum system can reach (Landauer resistance  $R = h/2e^2 \approx 13 \text{ k}\Omega$  for spin degeneracy and one occupied level) [50]. As can be deduced from Figure 34 (left), the voltage gain of this device is approximately 3.

By combining an odd number of inverter elements and feeding the output back to the input it was possible to realize a ring oscillator, as shown in Figure 35. As indicated by the output oscillations the ring oscillator operates at a frequency of 5 Hz. The low frequency is obviously due to the parasitic capacitances and the high series resistances of the nanotubes which can at least partly be reduced by a complete integration of all components on the substrate.

The realization of simple logic circuits represents a giant step towards the integration of carbon nanotubes. This proof of their operation further enhances the thrust driving CNT technology forward. However, it should be noted, that the circuits realized up to now were build out of p-type transistors and the only complementary gate was realized by Derycke et al. [64].

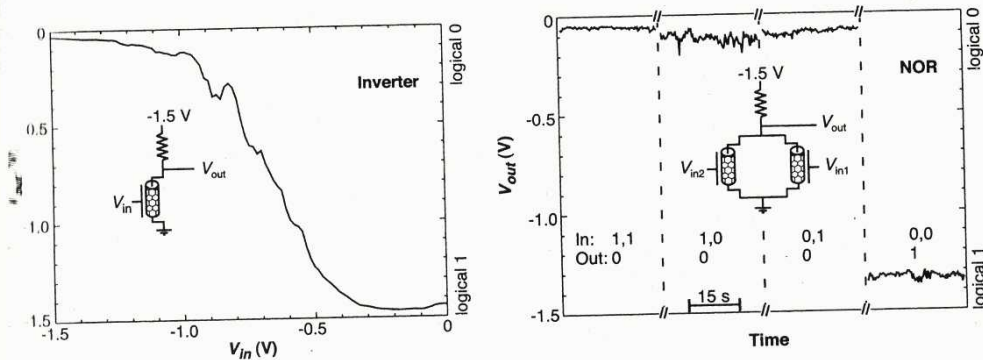


Figure 34: Left: The input-output characteristics of an inverter stage realized by a CNTFET and an external resistor. Right: Two CNTFETs in parallel working on a common resistor. Input/output characteristics showing NOR Function (taken from [65]).

## 6 Nanotubes for Memory Applications

Memory devices for information storage play a dominant role in microelectronics applications. The most important characteristics of a state-of-the-art memory concept are high storage density, fast and random data access, low power consumption, low price per bit, easy integration into the mainstream IC technology, and preferably non-volatility of data after power-off. For the Si technology, this has been achieved through devices such as DRAM, SRAM, EPROM etc. which are reviewed in Introduction to Part IV. In the following sections, we will address some of the first attempts to realize memory devices with carbon nanotubes.

### 6.1 CNT-SRAMs

It has been shown in Section 5.8 that basic circuits can be built with nanotubes. Once having realized a NOR gate, it is possible, by adding another resistor and cross-coupling the outputs to the inputs, to build up a simple SRAM unit-cell, as shown by the insert in Figure 36. Static memory function was demonstrated by writing a logical 1 or a logical 0 to the input, disconnecting the input voltage and tracing whether the output retained its logical state.

### 6.2 Other Memory Concepts

In principle, every information storage concept that exploits switching devices can also be realized with elements based on CNTFETs, as described in the previous section. However, it is challenging to look for new memory concepts which incorporate the specific characteristics of this macromolecular device in a more beneficial way. Such an attempt has been made by the Harvard University group of Lieber [69]. Their basic arrangement is a cross-bar array of carbon nanotubes with one set of nanotube wires separated from the other by a small distance provided by non-conducting supporting blocks (Figure 37).

It can easily be seen from Figure 38 that, for an optimum initial wire separation ( $\sim 2$  nm), the upper wires have two stable positions, one in their minimum elastic energy positions without contact to the lower cross-point wires and the other one with the wires held in contact with the lower wires due to the van der Waals force (left dip). If the contact state is reached, the electrical resistance of the cross-point changes by orders of magnitude. This can be detected by a sensing matrix and be exploited for bit storage. Once in the contact state, the wires can only be driven apart by charging them transiently with the same potential. Thus, we have a nonvolatile memory device that retains its memory information after power turn-off. The minimum cell size depends on the elastic deformation potential of the nanotubes including their suspension. The authors estimate the minimum cell size to be a square of 5 nm length, enabling a packing density of  $10^{12}$  elements/cm<sup>2</sup>. The inherent switching time was estimated to be in the 100 GHz range. The bending of the nanotube does not exceed the elastic limit and reversible switching operation of an experimental crossbar device was sustained over several days.

Another, and much more speculative, nano-mechanical memory principle is proposed in [70] where a charged bucky ball incorporated into a short carbon nanotube is driven into two stable sites at both ends of a very short tube by an electrical field applied

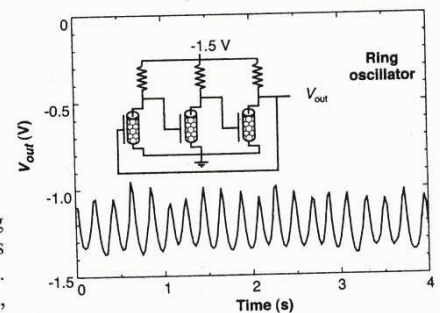


Figure 35: Combining an odd number of CNTFET NOR gates and feeding the output back to the input yields a ring oscillator. Oscillation of the output voltage is demonstrated. However, due to the high capacitances and resistors involved the frequency is very low (taken from [65]).

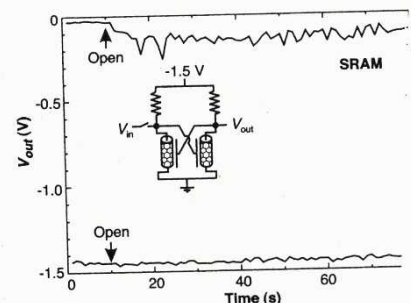
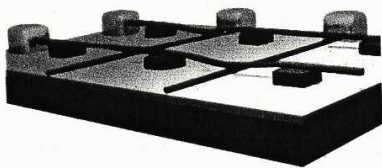
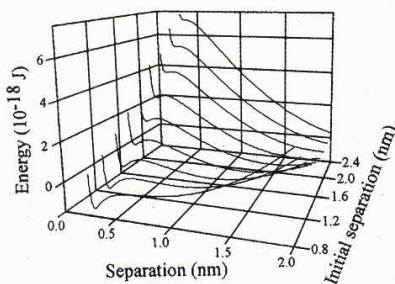


Figure 36: A simple SRAM cell made by two cross-coupled CNTFETs with external resistors. Writing either 1 or 0 to the input and disconnecting the input shows that the output remains in the stored state (taken from [65]).

## II Logic Devices



**Figure 37:** Crossbar arrangement of rows and columns of nanotubes separated by supporting blocks. Application of an appropriate voltage between the desired column and row bends the top tube into contact with the bottom nanotube. The resistance drop is used for bit storage. Van der Waals forces maintain the contact even if the voltage is removed (after [69]). Separation of the CNTs is achieved by application of a voltage pulse of equal polarity at the crossing point.



**Figure 38:** Total energy of the crossbar CNT memory cell system as a function of the initial tube separation (after [69]). For a distance of approx. 2 nm two minima can be realized representing the two stable configurations: contact (left minimum) and non-contact (right minimum).

**Figure 39:** A bucky ball incorporated in a short closed carbon nanotube (right). The Van der Waals forces favor two stable positions at both ends of the tube (left) which can be exploited for bit storage. The bucky ball is positively charged by the incorporation of a potassium ion (after [70]).

along the tube (Figure 39). A nonvolatile memory element can be constructed with this *bucky shuttle* device as memory node between an array of crossed lines. So far there is no report of a functional device based on this idea.

Following the principle of EEPROM memory, the authors of [71] propose to build a nanotube memory by combining semiconducting and metallic nanotube species in a crossbar configuration with a dielectric layer capable of storing charge in between. Each crossing point represents a transistor with gates formed from sections of the metallic tubes on top and the channel represented by the underlying section of the semiconducting tubes (Figure 40). By applying a high enough voltage at a cross-point, charges are induced into the  $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$  (ONO) dielectric and are trapped in the nitride, modifying the threshold voltage of the transistor. The threshold voltage shift is used to represent the two logic states. As all transistors are connected in series, NAND operation is favorable. First realization of this principle using an ordinary gate and a one layer  $\text{SiO}_2$  dielectric was achieved by Fuhrer et al [72]. They succeeded in reversibly injecting electrons from a nanotube into the gate dielectric. This extra charge shifted the threshold voltage of a CNTFET, which could be exploited for memory operation.

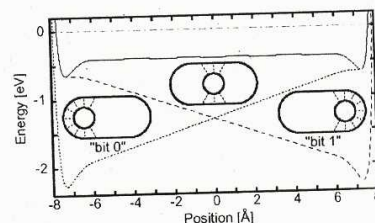
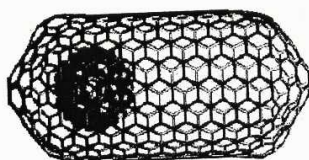
Information storage in nanotube devices undoubtedly seems to be attractive because the storage node can be scaled down to molecular dimensions and the inherent switching times are estimated to be extremely fast. However, the storage elements have to be connected to standard microelectronic circuits to detect the stored information and the timing cycles also have to comply with this external logic. It should also be noted that, though placement of the nanotubes in regular crossbar arrangements might be easier than in random networks, a reproducible method of deposition compatible with microelectronics technology requirements still has to be demonstrated.

## 7 Prospects of an All-CNT Nanoelectronics

In the preceding sections we have reviewed some of the most outstanding achievements that have been made in the last couple of years in the use of carbon nanotubes for devices which are the essentials of today's microelectronics: interconnects, transistors and even simple logic circuits and memories. We have also shown that these devices can compete with silicon devices or perform even better if we compare them at the appropriate length scale. It is therefore possible to conceive of a scenario in which all necessary elements of a functional microelectronics technology are made out of carbon nanotubes. For the moment we do not care that the most successful processing principle in silicon technology, i.e., the parallel processing of a great number of devices at the same time, has not yet been demonstrated for carbon nanotubes.

By assuming that it is possible to deposit the nanotubes with the desired characteristics on top of an arbitrary flat insulating substrate, one can imagine the integration scheme which is shown in Figure 41. Transistors as well as interconnects are made from the same multi-wall nanotubes with some sections being semiconducting and others being metallic. The semiconducting sections may be formed by controlled shell removal, as described in Section 5.2 until the desired characteristics are realized. Doping tube sections through a mask [63] would deliver the prerequisites for complementary devices. Even gate electrodes may be formed by the tips of nanotubes or by short sections of tubes lying parallel and close to the semiconducting ones.

Gate oxides and passivation layers may be deposited by conventional  $\text{SiO}_2/\text{Si}_3\text{N}_4$ -CVD, because nanotubes can withstand temperatures of more than  $1000^\circ\text{C}$  in inert atmosphere and  $\sim 400^\circ\text{C}$  in oxygen. Chemical mechanical polishing would flat-



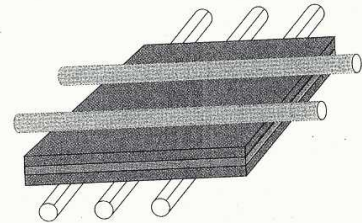
ten the surface allowing the stacking of more layers. Interconnects between the layers may also be constructed from nanotubes by exploiting the growth methods in vias described in Section 4.1. Thus, it would be possible to stack the desired number of layers by application of the processes already developed for semiconductor interconnect technology without the need for additional expensive processes for bonding prefabricated silicon chips on top of each other [73].

The ultimate step forward would be that, instead of exploiting the defect-free single crystal silicon surface for transistors, the nanotubes themselves provide the translational symmetry and quasi-crystalline perfection at the places we like to have it, and not just restricted to the silicon surface. Even wires would benefit from the crystalline structure, since surface and grain-boundary scattering is absent and electron-phonon interaction is low due to one-dimensional effects. The current carrying capacity is, therefore, orders of magnitude higher than in conventional metallic wires. The resistance of the wires would be independent of the length, provided that the large electron-phonon scattering length is not surpassed. The thermal conductivity of nanotubes is also higher so the nanotube network itself can act as an efficient heat transportation system.

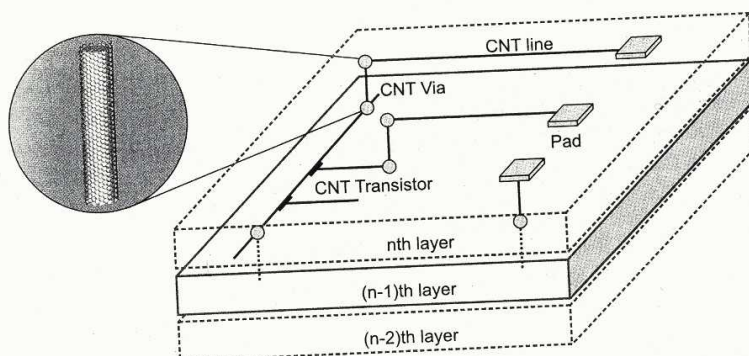
However, there is still a long way to go before this scenario can be realized, because a controlled parallel deposition of carbon nanotubes on a flat surface has not yet been demonstrated. On the other hand, it is well known that nanotubes can be considered as macromolecular structures and the deposition of certain predefined tubes might also be achieved using assembly methods derived from chemistry. Nanotubes can be functionalized with certain reactive groups [74]. If these groups are attached, e.g., to the ends of a semiconducting tube, it might be feasible to react them with appropriate molecules attached to specific sites on the substrate or to other nanotubes. After reaction the tubes may be coupled to other tubes or to predefined sites. Definition of the reaction site may be performed with lithographic methods. It can easily be imagined that, with this method, devices like CNTFETs or even circuits with interconnects might be constructed.

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**Figure 40:** Crossbar arrangement of semiconducting (bottom) and metallic (top) nanotubes separated by an ONO dielectric. Each crossing point represents a CNTFET. Application of a sufficient voltage at a node drives carriers into the ONO dielectric where they are trapped in the nitride causing a threshold voltage shift in the transistor. This is used as bit storage principle.



**Figure 41:** Concept for an all-CNT-based microelectronics technology. All active elements and interconnects are made out of nanotubes. Due to the quasi-crystalline nature of the nanotubes high quality devices are possible without the need for a single crystal silicon substrate. By the application of well known back-end-of-line techniques cost-effective stacking of a real 3-dimensional structure is feasible.



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